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Modelling and Comparative THD Analysis of Cascaded H-Bridge Multi-Level Inverters

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ABSTRACT:
Multilevel Inverters in recent years have more development and deployment in different industrial applications. Moreover, more research is being done on multilevel inverters by developing different switching and constructional topologies to get more power quality for DC-AC appliances. Total Harmonic Distortion is one of the major aspects in power quality. In this paper cascaded H-bridge with three, five, seven and nine level multilevel inverters are modelled. Sinusoidal Pulse Width Modulation (SPWM) technique is used as a control methodology for all the cascaded H-bridges modelled. Analysis of total harmonic distortion is done by using Fast Fourier Transform, where the nine-level cascaded H-bridge multilevel inverter has less harmonic distortion than the other three. Simulation is done, the results are obtained on MATLAB\Simulink software and a comparative analysis is done among the four different level inverters.
Keywords:*Multilevel Inverters, Cascaded H-bridge Multilevel Inverters, Total Harmonic Distortion, Control Methodology, Sinusoidal Pulse Width Modulation (SPWM), Comparative Analysis, MATLAB/Simulink.*

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I. INTRODUCTION

Inverters were developed in three categories based on motor drives, power supply and active filters. Among these Multilevel Inverters (MLIs) are treated as the preferred choice for academia and industries due to their high-power application capability. Multilevel Inverters were first introduced in the year 1975, which have come from three-level inverter. Basically, MLI, a power electronic device that gives the desired waveform of the output voltage as several levels of dc input voltages. It is because as the number of input dc voltage sources increases the output voltage becomes sinusoidal by fundamental frequency switching mechanism. The voltage stresses on the switching devices is less than the on overall operating voltage. Nowadays MLIs have small, medium and high power range applications.

H-bridge series design is the first topology for MLIs, following H-bridge, Diode Clamped topology has been developed. In diode-clamped topology, series capacitor banks are used to split the DC bus voltage. Later on Capacitor Clamped (flying capacitor) topology is used instead of series capacitors to clamp dc voltage at various levels. Researchers have also developed another design of MLIs, which comprise parallel connected inverters through interphase reactors. Various fundamental topologies cascaded to form hybrid topologies, which help to the improvement in power quality due to the multiplying effect of levels number that the fundamental topologies. Soft-switching schemes developed can also be used to reduce the switching losses, with obvious increase in efficiency [1-22].

Increase in power quality happens with reducing the Total Harmonic Distortion (THD) in MLIs as it lessens the lower level harmonics with a multi-stepped output waveform. In addition to THD, reduction in dv/dt stress and electromagnetic compatibility and stress reduction on drive bearings. One of the main disadvantage in MLIs is more switching devices are required. As the switching devices increase in number, the firing and control circuit becomes complex. Additionally, accumulation of voltage drop at each device can reduce the output voltage and higher power loss (heat loss) due to more switching devices.

This paper's aim is exhibit the advantage of reduction in THD with the increase in the levels of Cascading H-bridge MLIs. The paper is framed in a way that II section gives a brief description of MLIs. Following this, in III section control strategies of MLIs is described. Later on Simulation Results of the Cascaded H-bridge 3-level, 5-level, 7-level and 9-level are shown along with THD analysis in each.

II. MULTI-LEVEL INVERTERS

MLIs follows the arrangement of power switches like IGBTs/MOSFETs/Thyristors along with capacitor fed voltage sources. The common three types of MLIs are: (i) Diode/Neutral Clamped, (ii) Capacitor-clamped/Flying capacitors and (iii) Cascaded H-Bridge MLIs. Diode-clamped MLIs were introduced in 1981 by Nabae et al., where diodes are used to reduce the voltage stress, in which an n level inverter requires switching devices, input voltages and operating diodes of $(2n-2)$, $(n-1)$ and $(n-1)*(n-2)$ in number respectively.

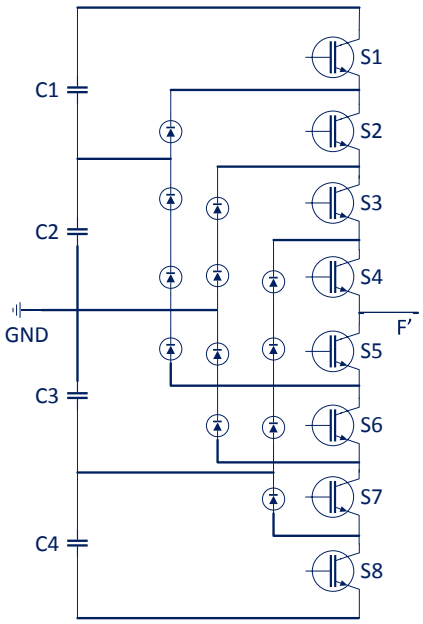

Figure 1. Circuit diagram of a diode-clamped MLI

However, in case of Capacitor-clamped MLIs, the voltage stress by controlled by capacitors instead of diodes in diode-clamped. An n level capacitor-clamped MLI must have switching devices and flying capacitors of $(2n-2)$ and $(n-1)*(n-2)/2$ respectively. The circuit diagrams of diode-clamped and capacitor clamped are given in the Figure.1 and Figure.2.

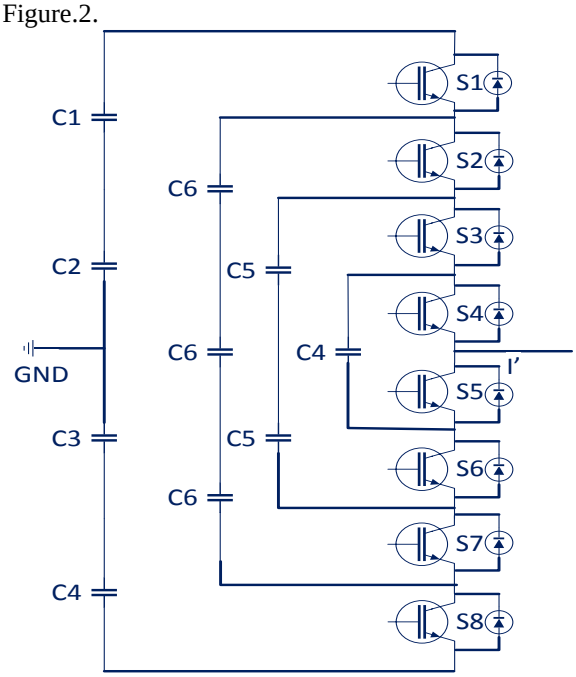

Figure 2. Circuit diagram of capacitor-clamped MLI

2.1. Cascaded H-Bridge Inverters

H-bridge is nothing but a single-phase full bridge inverter with four switching devices and a separate DC voltage source. Generally a H-bridge can generate voltage levels of $-V_{dc}$, 0, $+V_{dc}$ by considering different combinations of switches. When two diagonal switches are on the output is $+V_{dc}$ and if the other two switches are switched on the output is $-V_{dc}$. If all the switches are switched on simultaneously, the output voltage is zero. Figure 3 shows a single H-bridge inverter and Figure 4 shows the output waveform of the H-bridge inverter.

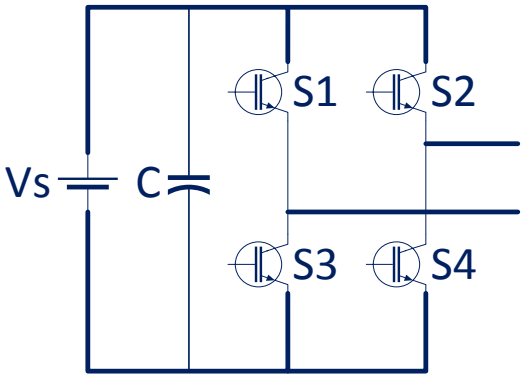

Figure 3. Circuit diagram of H-bridge inverter

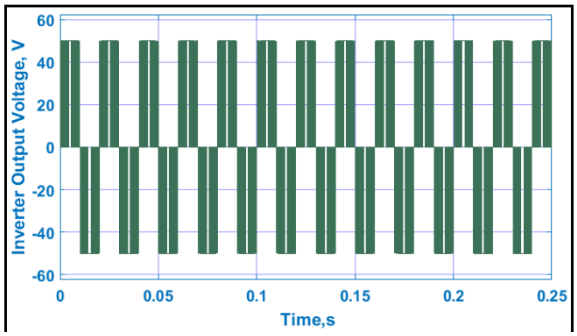

Figure 4. Three-level output voltage/output voltage of a single H-bridge

Cascaded H-bridge inverters, the name itself says that H-bridges are cascaded in such a way to get only the desired fundamental component of output voltage with less THD. Each H-bridge is considered as a cell.

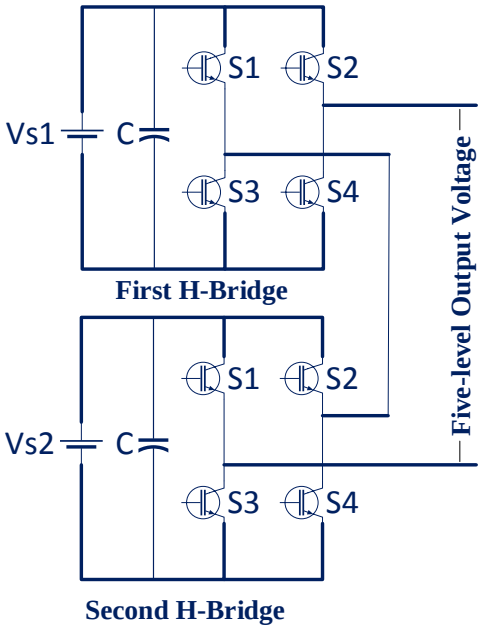

Figure 5. Five-level cascaded H-bridge inverter

The output voltage is nothing but the addition of inputs to all the cells. If the number of cells are n, then the levels in the output voltage is given by $(2n + 1)$. These have less components when compared to diode-clamped and capacitor-clamped MLIs.

III. CONTROL STRATEGIES OF MULTI-LEVEL INVERTERS

The control strategies in MLIs is nothing but the firing circuits for the power switches of the inverter. In case of cascaded H-bridge inverters many topologies have come into application. The most discussed multilevel modulation techniques are of three kinds namely, carrier-based Sinusoidal Pulse Width Modulation (SPWM), selective harmonic elimination and space-vector pulse width modulation. In this paper a carrier-based SPWM is used as a control strategy as it is proven advancement.

3.1. Sinusoidal Pulse Width Modulation (SPWM)

Multilevel Inverters using SPWM with triangular signal as the carrier signal and the reference signal as sinusoidal waveform. In case of an multi SPWM, the carrier signals are more than the basic SPWM For an m-level MLI the number of carrier signals required are $m - 1$. On comparing the multi-carrier signals with one reference sinusoidal signals gives pulses in a way to get less THD.

Multiple carrier signals used in MLI are either vertically shifted or horizontally shifted, as pulse generation is easy on a digital computer or the number of a times a module can switch on and off is constant respectively. However, there comes three variants of vertical shifting methodologies:

(i) PH Disposition: All the multi-carriers are in phase

(ii) PO Disposition: The carriers above the zeroth reference are in phase and the carriers below are in opposition with the above

(iii) APO Disposition: All are consecutively in opposition

IV. SIMULATION RESULTS AND DISCUSSIONS

The Simulation of modeling and harmonic analysis of Cascaded H-Bridge 3-level, 5-level, 7-level and 9-level inverters are done by using MATLAB\Simulink.

4.1. Analysis of Three-Level Cascaded H-Bridge Inverter

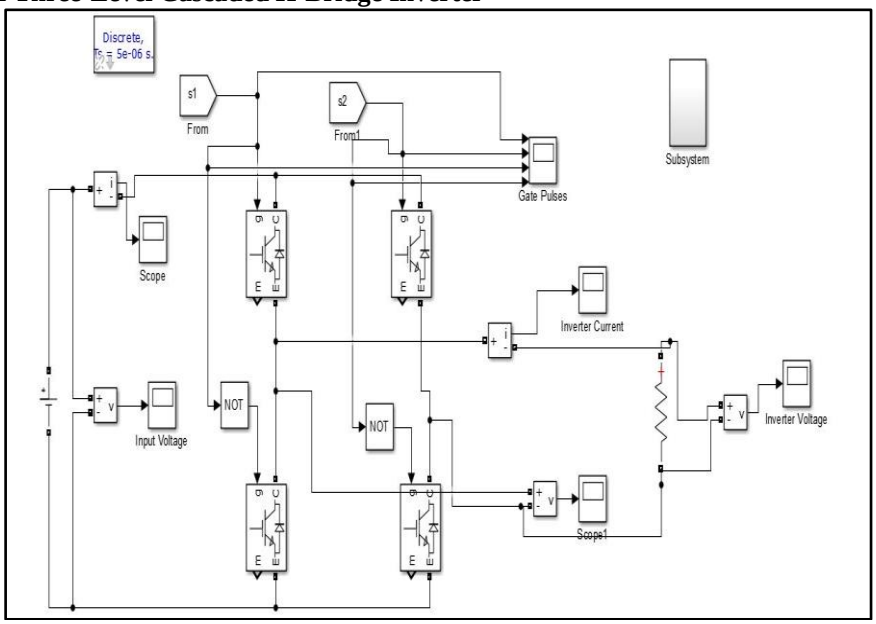

Figure 5. Simulation model of three-level single H-bridge inverter

In Figure 5, the simulation diagram of one H-Bridge Inverter is shown where it can give a 3-level 1-∅ output voltage. SPWM technique is used to obtain the gate pulses for the switches of a H-Bridge Inverter where gate pulses to the switches S_1, S_2 are the converse of gate pulses to the switches S_3, S_4. SPWM technique, a comparison of Sinusoidal and ramp (carrier) signal for switches S_1, S_2 is shown in Figure 6 and the gate pulses are shown in Figure 7.

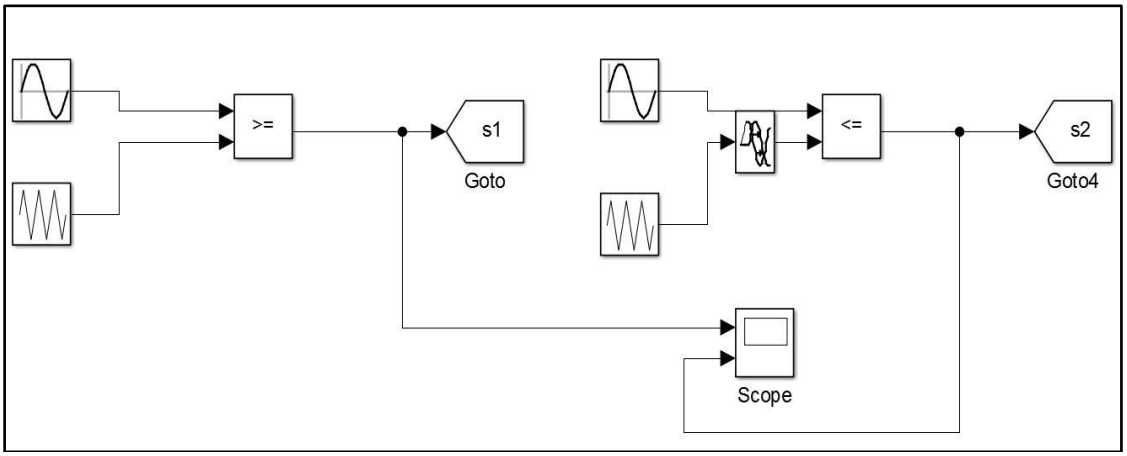

Figure 6. SPWM control strategy of single H-bridge inverter

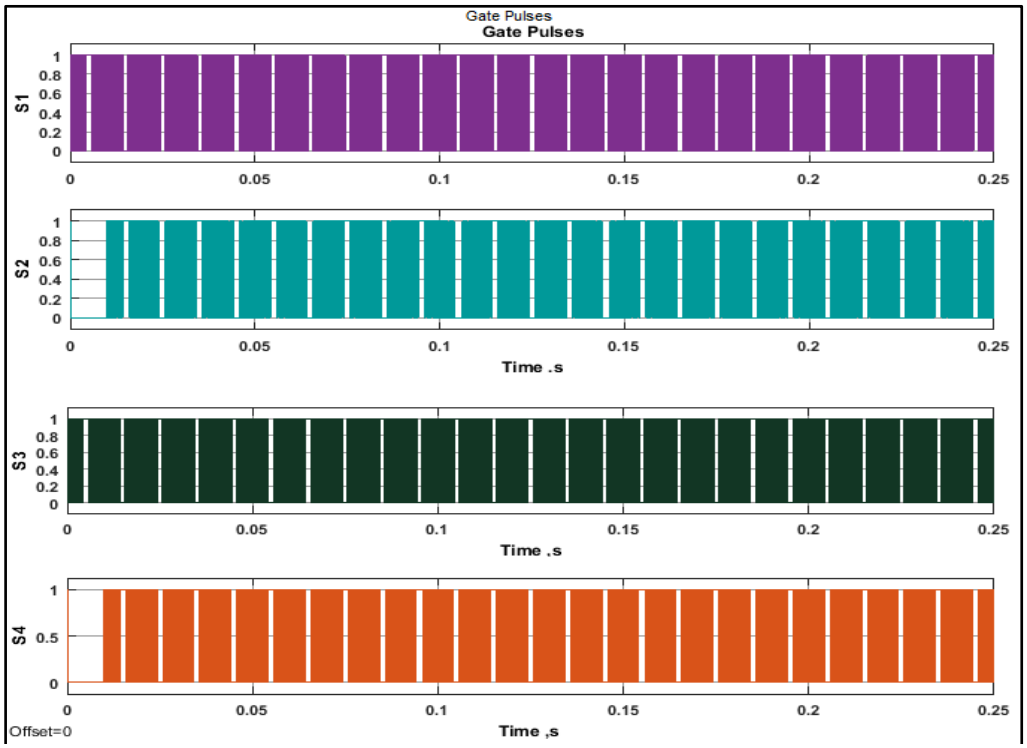

Figure 7. Gate pulses for switches S_1, S_2, S_3 and S_4

Figure 8 depicts the three-level Output Voltage across a 100Ω resistive load and Figure 9 shows the three-level inverter output current.

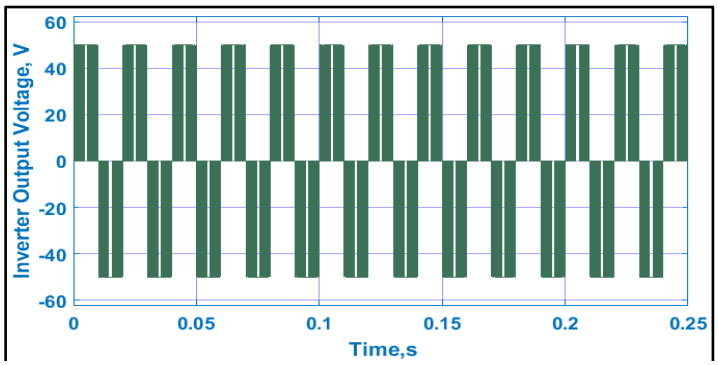

Figure 8. Three-level inverter output voltage

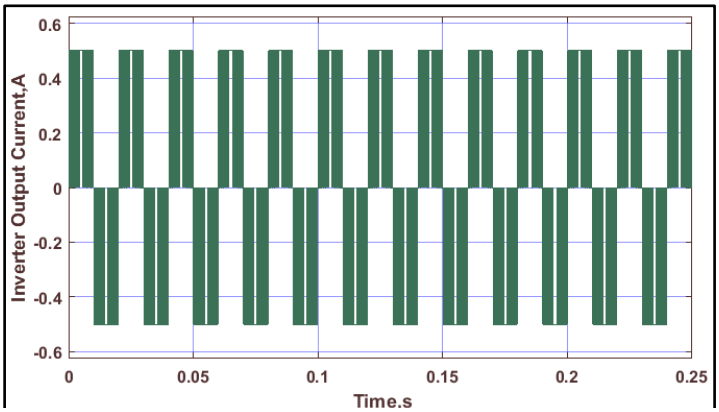

Figure 9. Three-level inverter output current

Three-level single H-bridge inverter Output Voltage waveform's THD analysis has been made Fast Fourier Transform (FFT) Analysis by using FFT analysis toolbox in MATLAB\Simulink. Harmonic level of the inverter output voltage is 52.12% is shown in Figure 10.

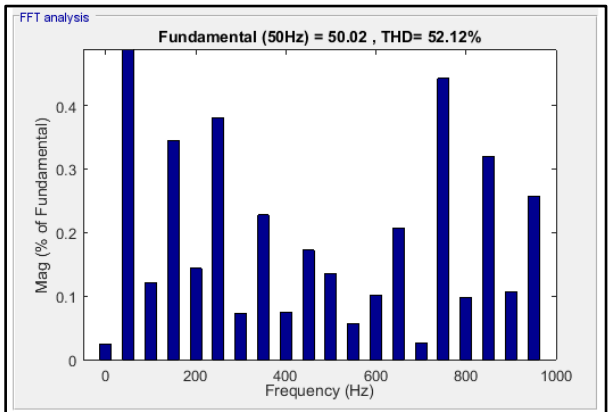

Figure 10. % THD of a three-level H-bridge inverter output voltage

4.2. Analysis of Five-Level Cascaded H-Bridge Inverter

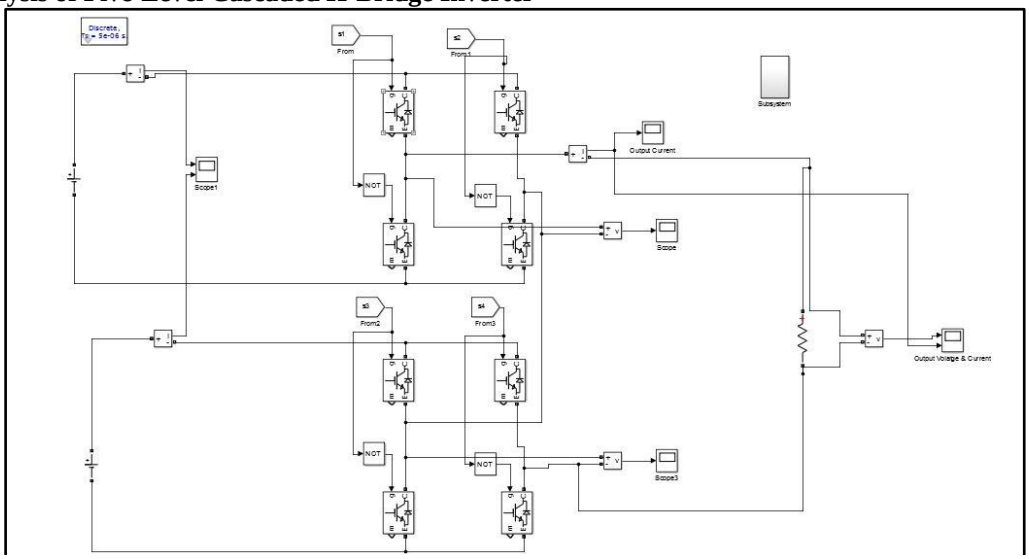

Figure 11. Simulation model of five-level cascaded H-bridge inverter

In Figure 11, the simulation diagram of five-level Cascaded H-Bridge Inverter is shown where it can give a five-level 1-∅ output voltage. SPWM technique, a comparison of Sinusoidal and ramp (carrier) signal for switches S_1, S_2 is shown in Figure 12.

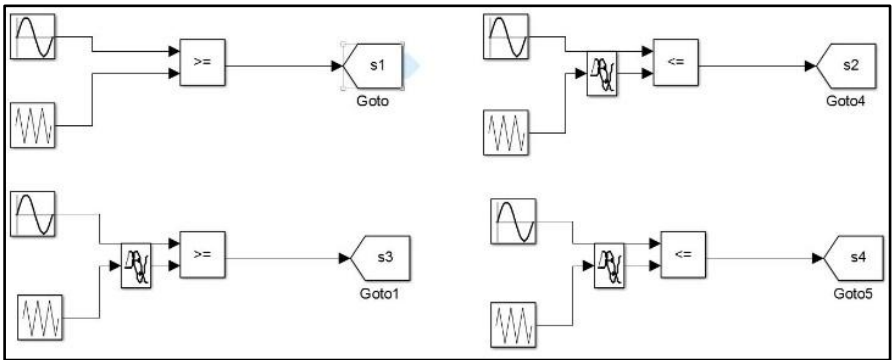

Figure 12. SPWM control strategy of five-level cascaded H-bridge inverter

Figure 13 depicts the 5-level Output Voltage across a 100Ω resistive load and 5-level inverter output current.

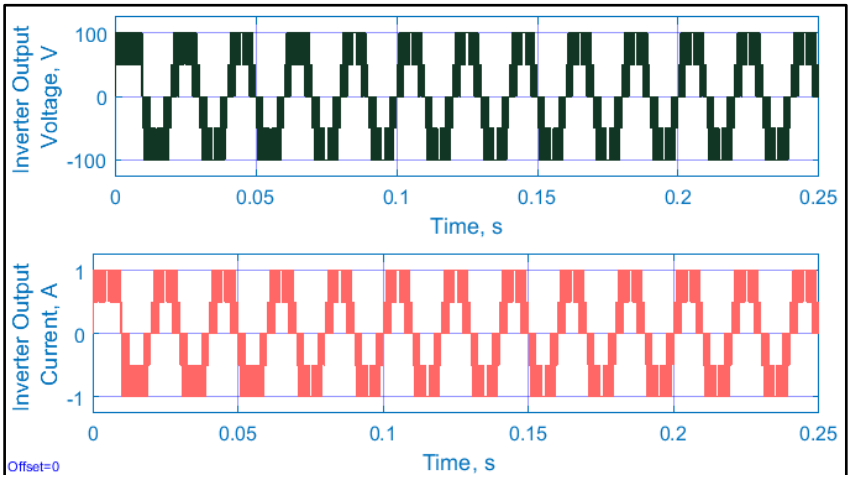

Figure 13. Five-level inverter output voltage and output current

Figure 14 depicts the Input current waveforms of first and second H-bridges consecutively.

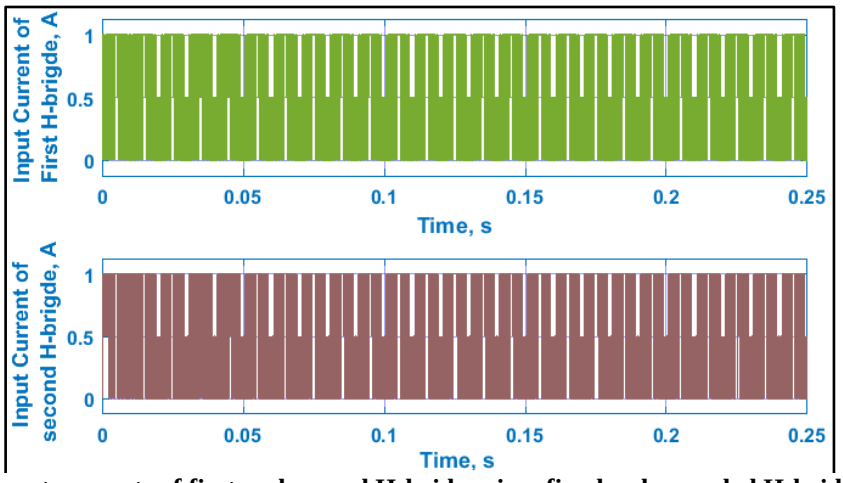

Figure 14. Input currents of first and second H-bridges in a five-level cascaded H-bridge inverter

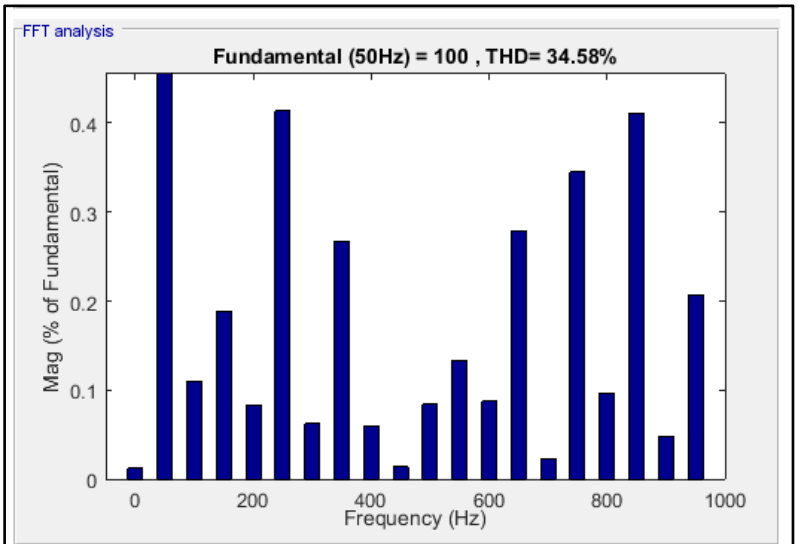

Figure 15. % THD of a five-level cascaded H-bridge inverter output voltage

Five-level cascaded H-bridge inverter Output Voltage waveform's THD analysis has been made Fast Fourier Transform (FFT) Analysis by using FFT analysis toolbox in MATLAB\Simulink. Harmonic level of five-level cascaded H-bridge inverter output voltage is 34.58% is shown in Figure 15.

4.3. Analysis of Seven-Level Cascaded H-Bridge Inverter

Figure 16 depicts the Seven-level Output Voltage across a 100Ω resistive load and seven-level inverter output current.

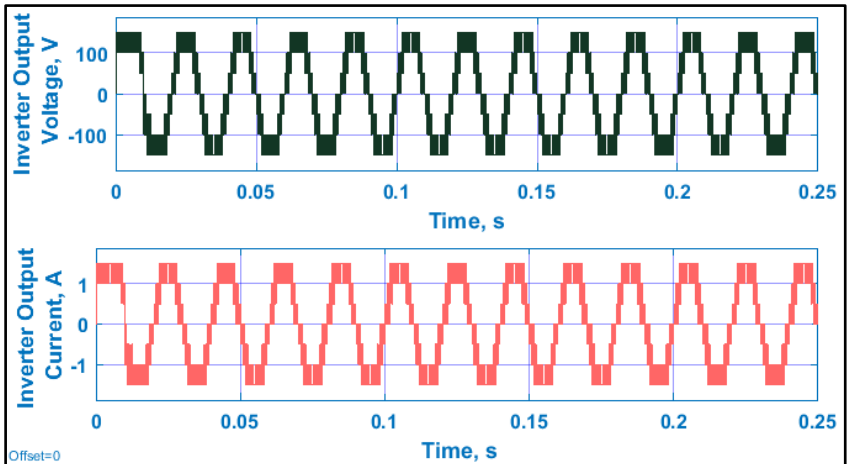

Figure 16. Seven-level inverter output voltage and output current

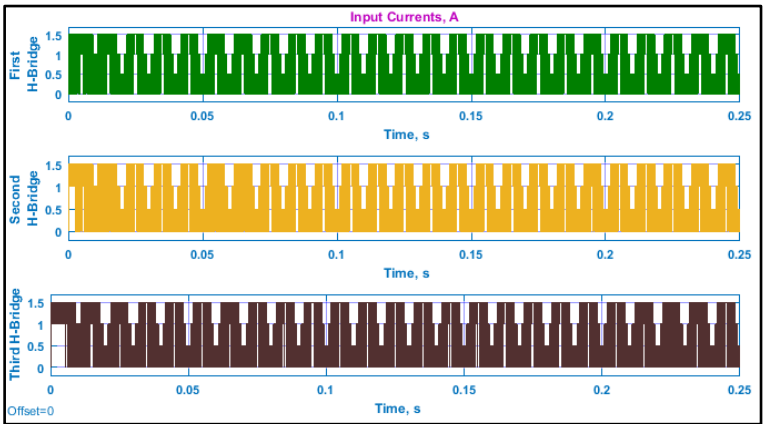

Figure 17. Input currents of first, second and third H-bridges in a seven-level cascaded H-bridge inverter

Figure 17 depicts the Input current waveforms of first, second and third H-bridges consecutively.

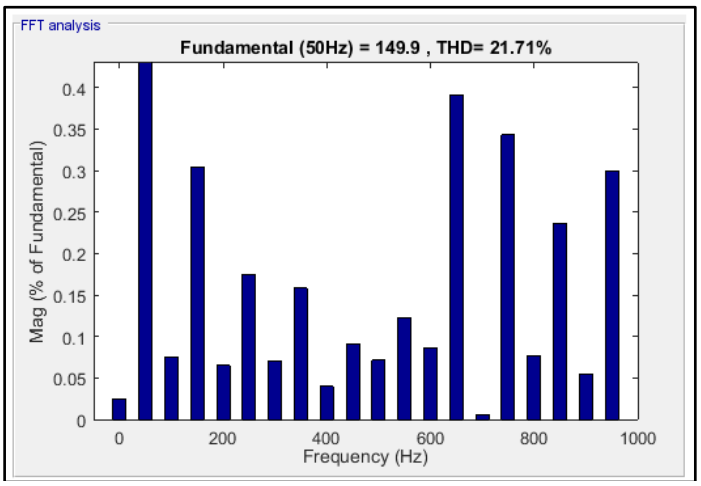

Figure 18. % THD of a seven-level cascaded H-bridge inverter output voltage

Seven-level cascaded H-bridge inverter Output Voltage waveform's THD analysis has been made Fast Fourier Transform (FFT) Analysis by using FFT analysis toolbox in MATLAB\Simulink. Harmonic level of seven-level cascaded H-bridge inverter output voltage is 21.71% is clearly shown in Figure 18.

4.4. Analysis of Nine-Level Cascaded H-Bridge Inverter

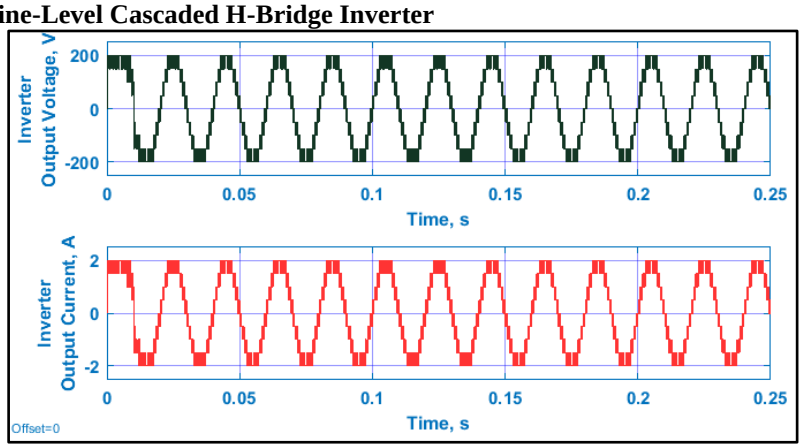

Figure 19. Nine-level inverter output voltage and output current

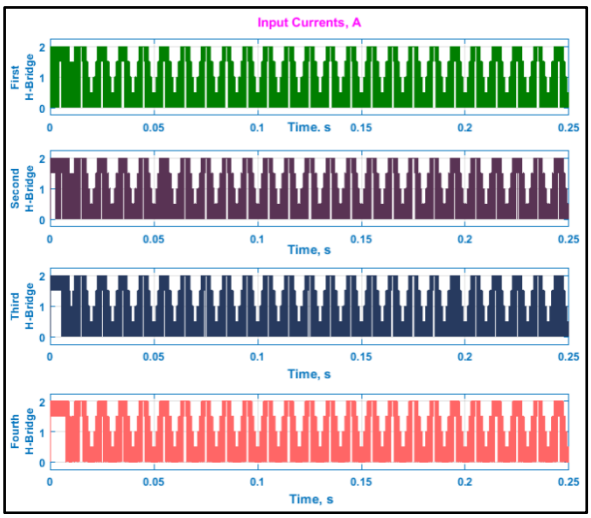

Figure 20. Input currents of first, second, third and fourth H-bridges in a nine-level cascaded H-bridge inverter

Figure 19 depicts the Nine-level Output Voltage across a 100Ω resistive load and nine-level inverter output current. Figure 20 depicts the Input current waveforms of first, second, third and four H-bridges consecutively. Nine-level cascaded H-bridge inverter Output Voltage waveform's THD analysis has been made Fast Fourier Transform (FFT) Analysis by using FFT analysis toolbox in MATLAB\Simulink. Harmonic level of nine-level cascaded H-bridge inverter output voltage is 13.83% is clearly shown in Figure 21.

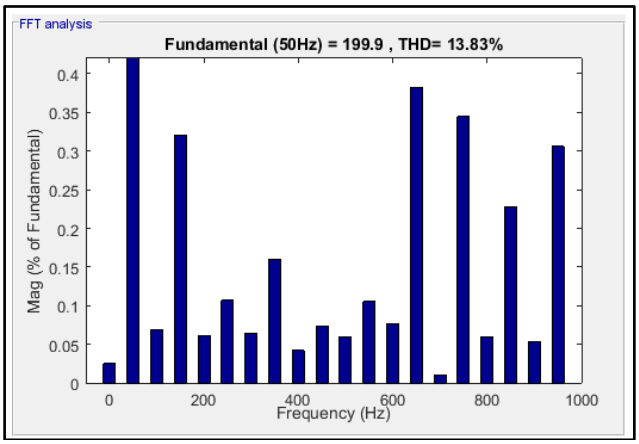

Figure 21. % THD of a nine-level cascaded H-bridge inverter output voltage

The overall analysis of three-level, five-level, seven-level and nine-level cascaded H-Bridge inverters is shown on the Table 1. Hence it is clear that as if the levels of H-bridges are increased then THD reduces. But if the levels are more, gate firing becomes complex. So it is better to select an optimal number of H-bridges while designing a cascaded H-bridge MLI.

Table 1. Overall analysis of cascaded H-bridge inverters

Inverter Level Type	Input Voltage	No. of H-Bridges	Switch Type	Total no. of Switches	Output Voltage	THD, %
Three	50	1	IGBT	4	50	52.12
Five	50+50	2	IGBT	8	100	34.58
Seven	50+50+50	3	IGBT	12	150	21.71
Nine	50+50+50+50	4	IGBT	16	200	13.83

V. CONCLUSION AND FUTURE SCOPE

In the presented thesis, modelling of three-level, five-level, seven-level and nine-level Cascaded H-bridge multi-level inverters is done. Cascaded H-bridge MLIs are more advantageous than diode-clamped and capacitor-clamped MLIs. One cascaded H-bridge circuit with four switches act as a three-level inverter. The four switches in each H-bridge are controlled by SPWM control strategy. Therefore, two H-bridges, three H-bridges and four H-bridges (in cascade) are required to obtain five-level, seven-level and nine-level inverters respectively. For input DC voltage of 50V, applied to each H-bridge, frames a symmetrical MLI. Simulation modelling of all the four levels of MLIs is done as shown in figures of Section 4. Table 1 shows the consolidated THD values of all the four different levels of inverters. Among the four, nine-level MLI, which require four Cascaded H-bridges gives a less THD value of 13.83% than the other three.

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