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# Design and Analysis of Energy Efficient MOS Digital Library Cell Based on Charge Recovery Logic

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***ABSTRACT:*** *Recent trends in CMOS VLSI design are reducing MOSFET size continue in terms of channel length for small IC and due to this, the major issue of energy dissipation is the subject of worry. For resolve this, an idea of reversible logic is introduced for getting low power and high-speed switching in CMOS logic circuits, which reduces the power dissipation by reusing the energy drawn from the power supply. In this paper, 70 nm technology model file available from predictive technologies is used to simulate results for proposed logic and other strategies. These results show empirical comparison between different parameters such as logic style, power dissipation and delay and illustrate the proposed logic cell has significant improvement in terms of power dissipation. These improvements show that proposed method can considerably reduce the power consumption in new design when compared to the conventional CMOS design techniques.*
***KEYWORDS****: Reversible logic, charge recovery, Low power, Power clock*

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## I. INTRODUCTION

VLSI designers have been motivated to explore new ideas in the field of VLSI design for low power and high-speed digital circuits. The thermal stress caused by power dissipation as heat, on chip is a major issue. So, reduction of power dissipation is also desirable for reliability. Reversible logic is a promising approach, which has been originally developed for low power digital circuits [1]. At the time of switching activity, dynamic power dissipation is a dominant factor. In conventional CMOS circuits, energy dissipation can be minimized using reversible logic and some of energy stored in load capacitance can be reused instead of dissipated as heat [2].

There are some traditional approaches to reduce the dynamic power dissipation such as decreasing voltage power supply, reducing physical capacitance and reducing switching activity [3]. These techniques are old and not enough to meet desired power requirement in present condition. Hence, most research has been focused on building adiabatic logic. Adiabatic logic works with switching activities which reduces the power by giving stored energy back to the supply [4]. Hence, the term adiabatic is relevant for low power VLSI design circuits, which implements reversible logic. Generally power supplies of adiabatic logic circuits have used constant current source, while non-adiabatic circuits that have used fixed-voltage power supply.

## II. COMPONENTS OF POWER DISSIPATION

i) Dynamic (switching) power dissipation: When charging or discharging of the parasitic capacitances occurs during a node voltage transition.

ii) Leakage power dissipation: Combination of MOSFET switches and gate leakage power caused by carrier tunneling through thin gate oxides.

iii) Short-circuit power dissipation: Transitory power dissipation during an input signal transition when both the pull-up and pull-down network of CMOS gate are simultaneously on.

iv) Static power dissipation: Static DC power consumed when a CMOS circuit is driven by low voltage swing input signals.

## III. DYNAMIC POWER DISSIPATION

Charge-up phase: Output voltage rises from zero to $V_{DD}$. Fifty percent of energy taken from supply is dissipated as heat through PMOS and rest is stored in load capacitance.

Charge-down: Output voltage drops from $V_{DD}$ to zero. Load capacitance energy is dissipated as heat through NMOS [5, 6].
General CMOS circuit having NMOS network, PMOS network and total output load capacitance is shown in Fig. 1 [2].

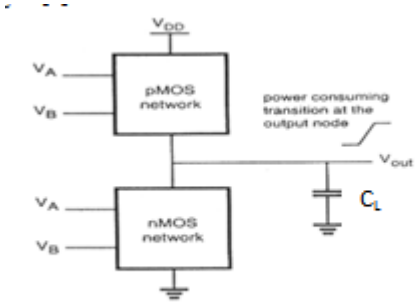


**Figure 1.** General CMOS circuit [2]

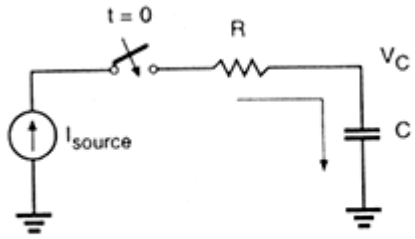


**Figure 2.** Equivalent circuit for adiabatic switching [2]

The average dynamic power dissipation for this network is given as:

$$P_{avg} = \left( \sum_{i=1}^{\#\ of\ nodes} \alpha_{Ti} C_i V_i \right) V_{DD} f_{CLK}$$

Where, $\alpha_T$ Switching probability, $V_i$ the node voltage, $V_{DD}$ the full voltage swing, $C_i$ is the parasitic capacitance linked with each node in the circuit ( including the output node ) and $\alpha_{Ti}$ represents the corresponding node transition factor associated with that node [2].

## IV. ADIABATIC LOGIC

In conventional CMOS logic circuits, each switching event causes an energy transfer from the power supply to the output node [2, 7]. In steady state, either PMOS network will be ON or NMOS network, it depends on input signal value. If an input signal switches from 1 to 0, A charge of $Q = C_{load}V_{DD}$ is occupied from the voltage source, an energy quantum of $E_{supply} = QV_{DD} = C_{load}V^2_{DD}$ is drawn from the power supply during this transition. The difference between the delivered energy and the stored energy is dissipated in the PMOS network. If an input signal switches from 0 to 1, in steady state, NMOS is on and PMOS is off. Then charge stored on load capacitance is dissipated through NMOS network to ground.
To minimize the power dissipation, we can reduce switching activities or load capacitance or voltage swing or apply a combination of these three. For making energy efficient logic circuits, the concept of adiabatic logic can be introduced for charge recovery [8, 9].
Fig. 2 shows a circuit for adiabatic switching where a constant current source equivalent to linear voltage ramp is used to charge the load capacitance instead of using constant voltage source. In circuit, resistance R is equivalent to the ON resistance of PMOS network. Charge can be transferred to the load capacitance through the power supply using constant current charging process. By adiabatic operation it is possible to allowing the stored charge from the load capacitance back to the power supply by reversing the current source direction. For this, constant current source must be capable to retrieve the energy from the load capacitance. Hence adiabatic logic circuits require pulsed power supply [2, 10].
The conventional CMOS logic gate and adiabatic logic gate are shown in Fig. 3(a) and Fig. 3(b) respectively. A conventional CMOS logic gate can be converted into an adiabatic logic gate. For this, pull-up and pull-down networks of the conventional CMOS logic circuits must be changed with complementary transmission gate networks [11].

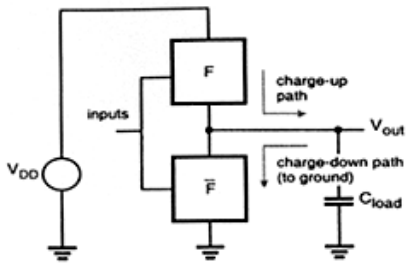


**Figure 3(a).** Conventional CMOS logic [2]

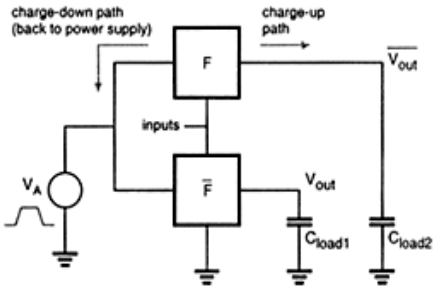


**Figure 3(b).** The topology of an adiabatic logic implementing the same function [2]

A CMOS inverter is shown in Fig. 4. This circuit uses a stepwise voltage ramp $V_A$ as a power supply having n equal voltage steps as shown in Fig. 5. When supply rises from zero to $V_{DD}$, the load capacitance is charged through a resister (ON resistance of PMOS) in small voltage increments. Therefore, the total energy dissipation (hence total power dissipation) is reduced by a factor using stepwise charging. If n approaches infinity i.e. if supply voltage is a slow linear ramp, the energy dissipation will approach zero.

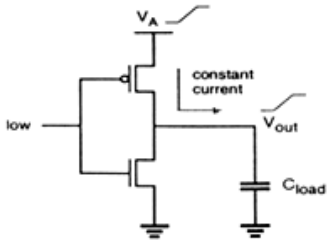


**Figure 4.** A CMOS inverter circuit with a stepwise increasing supply voltage [2]

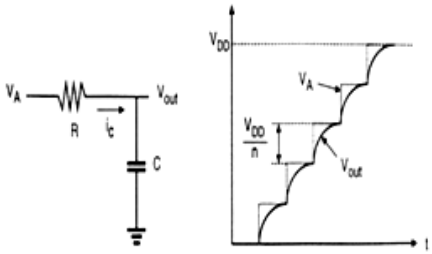


**Figure 5.** Equivalent circuits and the input and output voltage waveforms of the CMOS inverter circuit [2]

## V. DIFFERENT LOGIC FAMILIES

Practical adiabatic families can be classified as either partially adiabatic or fully adiabatic. In a partially adiabatic logic circuit, some charge is allowed to be transferred to the ground. In a Fully Adiabatic, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face problems with respect to operating speed and input power clock synchronization. Complete recovery of the power-clock is not possible through the PMOS device, so it is still only a quasi-adiabatic logic style [12].

### 5.1 Efficient Charge Recovery Logic (ECRL)

Fig. 6(a) shows the schematic of the Efficient Charge Recovery Logic (ECRL). A detailed description of ECRL can be found in [10, 13, 14]. Full output voltage swing is obtained because of the cross-coupled PMOS transistors in both, pre-charge and recover phases. But due to the threshold voltage of the PMOS transistors, circuit suffers from the non-adiabatic loss in both, pre-charge and recover phases.

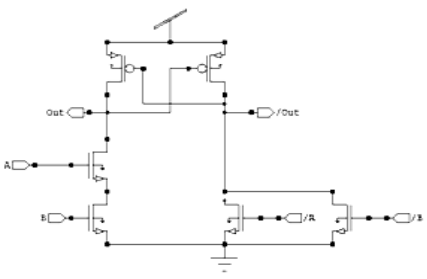


**Figure 6(a).** Structure of ECRL Logic

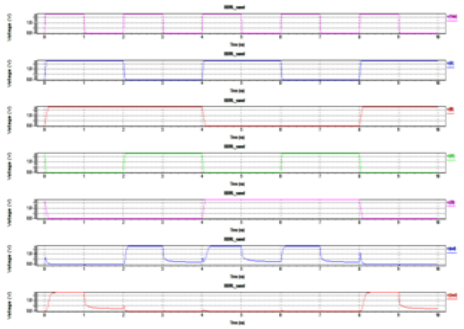

**Figure 6(b).** Simulated waveforms of ECRL

**5.2 Positive Feedback Adiabatic Logic (PFAL)**

Fig. 7(a) shows the schematic of the Positive Feedback Adiabatic Logic (PFAL). A detailed description of PFAL can be found in [9]. Here latch is made by two PMOS and two NMOS and functional block is in parallel with PMOSFETs, hence equivalent resistance is smaller at the time of charging the capacitance.

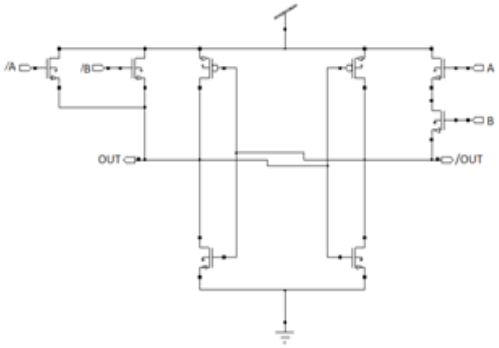


**Figure 7(a).** Basic Structure of the PFAL Logic

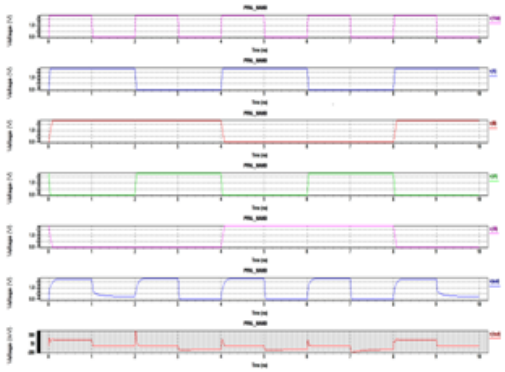

Figure 7(b). Simulated waveforms of PFAL Logic

**5.3 Proposed logic**

In CMOS circuits, active power dissipation depends on voltage swing, node capacitances and the switching activity of the circuit (number of transitions occurred per second) which depends on the frequency of operation. Fig. 8(a) shows the general schematic of the proposed logic. Proposed research work is based on circuit level approach to minimize power dissipation in MOS circuit, in which energy loss is reduced by limiting voltage differences across conducting devices. We ensure that the voltage drop across the transistor is relatively small at the time when the switching occurs. This is accomplished by using time varying voltage waveforms. A minimum dissipation of the energy at 500 MHz clock frequency is observed. Therefore, an optimum frequency exists in adiabatic logic, where energy consumed per cycle is minimum.

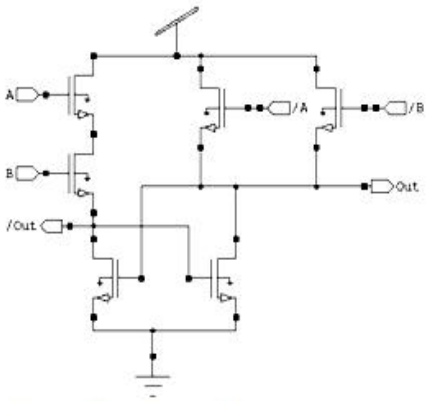


**Figure 8(a).** Proposed circuit

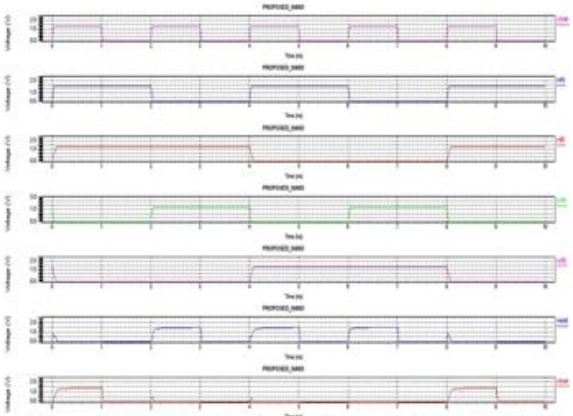

**Figure 8(b).** Simulated waveforms of proposed logic

## VI. RESULT AND DISCUSSION

The proposed logic circuit is designed using 70 nm PTM model file and is simulated using SPICE tool. Power clock supply is 1V. Evaluation of the performance of proposed architecture in terms of power consumption is given in table 1 and compare with other technology. Power consumed and delay by three technologies are shown in Fig. 9(a) and 9(b) respectively. The plot of power dissipation verses frequency shows that proposed logic gives better result in terms of power dissipation than ECRL and PFAL.

**TABLE 1**: POWER DISSIPATION

| Name/ Freq. | 50MHz | 100MHz | 200MHz | 250MHz | 500MHz |
|---|---|---|---|---|---|
| **ECRL** | 4.30E-07 | 7.90E-07 | 1.50E-06 | 1.90E-06 | 1.30E-06 |
| **PFAL** | 3.40E-05 | 3.50E-05 | 3.50E-05 | 3.50E-05 | 1.60E-05 |
| **PROPOSED** | 2.60E-07 | 4.40E-07 | 8.60E-07 | 1.00E-06 | 9.30E-07 |

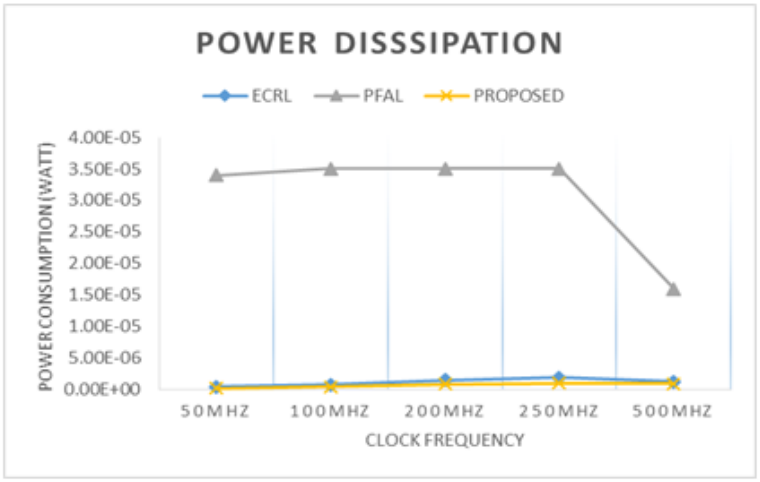


**Figure 9(a).** Comparative analysis of Power consumption

**TABLE 2**: DELAY

| Name/ Freq. | 50MHz | 100MHz | 200MHz | 250MHz | 500MHz |
|---|---|---|---|---|---|
| **ECRL** | 1.60E-10 | 1.00E-10 | 7.60E-11 | 2.00E-09 | 1.10E-11 |
| **PFAL** | 1.00E-11 | 7.10E-11 | 4.50E-11 | 4.50E-11 | 2.30E-10 |
| **PROPOSED** | 1.20E-10 | 7.90E-11 | 6.90E-11 | 2.00E-09 | 5.90E-11 |

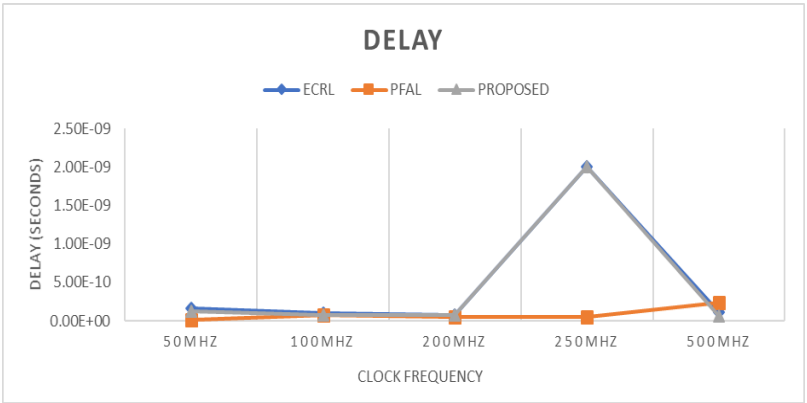


**Figure 9(b).** Comparative analysis for delay

## VII. CONCLUSION

In this paper energy efficient NAND gate based on ECRL, PFAL and proposed logic is presented. The proposed logic exhibits considerable improvement in terms of power dissipation and delay compared to ECRL and PFAL technology.

In summary, proposed logic can provide useful building block in design of energy efficient circuits.

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