ISSN (e): 2250 – 3005 || Volume, 08 || Issue, 05|| May – 2018 ||
International Journal of Computational Engineering Research (IJCER)

New Structure of Switched Capacitor MLI with Lessnumber of Device

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Abstract*—The aim of this paper is to present a novel structure of switched capacitor multilevel inverter (SCMLI) which can produce a great number of output voltage levels using a reduced number of components such as isolated dc power sources, switching devices, driver circuits, capacitors and power diodes. The proposed SCMLI can produce 13 output voltage levels and 21 output voltage levels by using symmetric and asymmetric dc source configuration respectively and 14 switches, 3 diodes and 3 capacitors. To enhance the output voltage levels, cascaded MLI structure using proposed basic SCMLI structure has been introduced. Further, the cascaded SCMLI has been analyzed for the symmetric and asymmetric dc source configurations. As compared to other topologies, the presented topology provides more output voltage levels using reduced components. In the comparison study, different aspects of the number of switches, dc power supplies, capacitors, diodes for producing specific output voltage levels are accounted. Further, the switching stress and Total Standing Voltage of the inverter has been determined and compared with that of other topologies. The extensive simulation study of the symmetric and asymmetric structure of proposed SCMLI have been done in MATLAB/SIMULINK under different condition. The simulation results provide the effectiveness of the proposed topology.*
Keywords*—cascaded MLI; capacitor voltage balance; switched capacitors; total standing voltage; voltage boosting*

I. INTRODUCTION

In recent years, multilevel inverter (MLI) becomes one of the most viable and crucial technologies in divergent applications such as renewable energy systems, motor drive applications, electrical vehicles, FACTS controller, HVDC applications, UPS systems, active filteringetc**[1]-[3]**. MLI has the ability to generate staircase or stepped output voltage waveform. Due to the staircase nature of the output waveform, the quality of output waveform improves and follows the near sinusoidal nature, thereby reducing the total harmonic distortion (THD). In comparison to the classic 2 level inverters, MLI offers numerous advantages such as improved output voltage, lower stress voltage across the switches, lower electromagnetic interference (EMI), more power handling capability.

Generally, MLIs are classified into three types namely neutral point clamped (NPC), flying capacitor (FC)and cascaded H bridge(CHB) **[4-6]**. In NPCMLI, the input voltage is divided into several low-value dc voltages by employing capacitors. The most distinctive feature of the diode clamped is its industrial applications due to simple structure and control. On the other hand, FCMLI is more flexible than the NPCMLI. Unlike NPCMLI, FCMLI uses capacitors to clamp the switch voltages. However, an increment in the number of levels leads to the rise in the number of clamping diodes in NPCMLI and capacitors in FCMLI, thereby incrementing the cost, complexity, and control and thus decreasing the overall efficiency of the circuit. CHB generates multilevel output waveform by adding/subtracting different dc voltage sources. This topology does not require any clamping diodes or flying capacitors. This topology is modular in nature and simple in structure. but the topology requires a large quantity of isolated input dc sources as the output level increases. To overcome the above-mentioned limitations of conventional MLI topologies, several new topologies have been developed in literature in recent years**[7]-[15].** Paper **[7-8]** present novel cascade MLIs satisfying the objective of reduced device count to generate a particular number of output voltage level. The limitation encountered in the proposed topology is the need fora large number of dc power sources. Paper **[9]** introduces an asymmetric Square T-type MLI. However, the limitation of high device count still pertains in this topology.

Switched capacitor multilevel inverters (SCMLIs) are one of the major fields in which recent advances have been made by the researchers. Switched capacitor MLIs utilize less number of isolated dc power sources in comparison to various developed MLI topologies. In other MLI topologies transformer is utilized to boost the output voltage. This, in turn, increments the cost and complexity and decrements the efficiency of the circuit. On the other hand, SCMLIs do not require a bulky transformer/inductors to boost the output voltage. Paper **[10]** presents a novel SCMLI which utilizes switched capacitor and an inherent H-bridge to produce both positive and negative voltage levels. A symmetrical triangular waveform modulation is implemented in this topology facilitating the operation of the proposed topology at high frequency. The only limitation that this topology depicts is increased component count with an increase in the output voltage levels. Paper **[11]** presents two new topologies of SCMLI. The proposed topologies employ both the conventional series and switched capacitor modules. However, in these topologies, one H-bridge is associated with each switched capacitor units. This leads to the increment of stress voltage across the switches and the switch count increases with voltage levels. Papers **[12]** present novel MLI topologies based on switched capacitor technique. The topologies utilizeone input voltage source and the complications in capacitor voltage balancing is also taken into consideration. However, a large number of capacitors and diodes are utilized at higher voltage levels, thereby increasing the component count. Papers **[13]-[15]** present SCMLI topologies, but the problem of increasing component count still exists.

In Section II, the basic unit is introduced and the switching table along with the load current path diagrams are mentioned. The algorithms for the source configuration is also mentioned. In Section III the proposed cascade topology based on basic units is introduced. In Section IV, comparison study is presented. In Section V, the simulation study in MATLAB/SIMULINK for different load condition are shown.

II. BASIC UNIT OF PROPOSED SCMLI

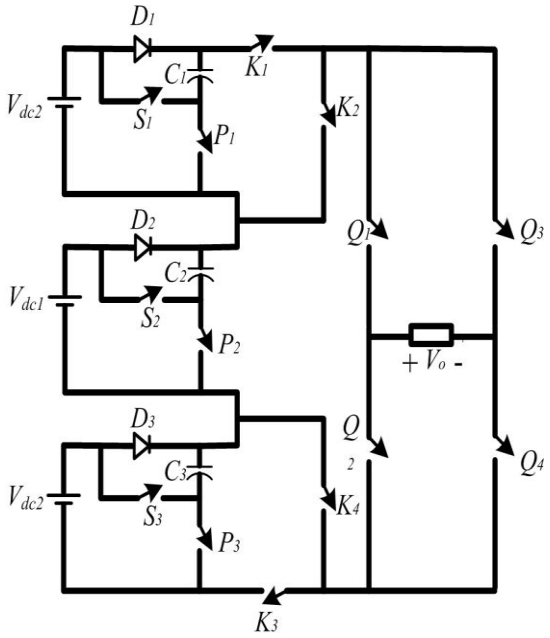

Fig. 1. Basic unit of the proposed topology

Fig. 1displays the basic unit of the proposed topology It generates 21 levels. This unit consists of 14 unidirectional switches. The basic unit is divided into two i.e. level generation (LG) part and polarity generation (PG) part. The LG part consists of three SC units and PG part comprisesan H-bridge circuit. The switches associated with LG part are S_1,S_2,S_3,P_1,P_2,P_3,K_1,K_2, K_3andK_4. The switches (S_1,P_1), (S_2,P_2) and (S_3,P_3) are the complementary pair of switches and hence, they cannot be switched on simultaneously as it would result in short-circuiting of the sources. The switches P_1,P_2,andP_3 connect the capacitor in parallel to the input dc sources leading to the charging of the capacitors. Once the capacitors are charged the switches S_1,S_2 andS_3 connect the capacitors in series with the input voltage sources enabling the discharging operation of the capacitors. When the capacitors are discharging the diodes D_1,D_2 andD_3get reverse biased and a voltage summation of the input voltages and the capacitor voltage is transferred to the output. The basic unit can be represented in both symmetric and asymmetric model.

Table I presents the switching sequence and the capacitor states for generating different voltage levels.where '+' and '-' represent charging and discharging state of the capacitor respectively. Further,NC stands for not connected condition of capacitors. Fig. 2 shows the equivalent circuits and current flow paths for different

output voltage levels. It can be inspected that there are two types of currents flowing in the circuit i.e. load current which is represented in the red line and the capacitor charging current for C_1, C_2, and C_3represented in the blue line.

TABLE I. ON SWITCHES CAPACITOR STATES FOR DIFFERENT OUTPUT VOLTAGE LEVELS

Output Voltage Levels	ON Switches	Capacitor State		
		C_1	C_2	C_3
$S_1,S_2,S_3,K_1,K_3,Q_1,Q_4$	$4V_{dc2}+2V_{dc1}$	-	-	-
$S_1,S_2,P_3,K_1,K_3,Q_1,Q_4$	$3V_{dc2}+2V_{dc1}$	-	-	+
$S_1,P_2,P_3,K_1,K_3,Q_1,Q_4$	$2V_{dc2}+2V_{dc1}$	+	+	-
$P_1,P_2,P_3,K_1,K_3,Q_1,Q_4$	$V_{dc2}+2V_{dc1}$	+	+	+
$S_2,P_1,P_3,K_2,K_4,Q_1,Q_4$	$2V_{dc1}$	+	-	+
$P_1,P_2,P_3,K_2,K_4,Q_1,Q_4$	V_{dc1}	+	+	+
$Q_1,Q_4/Q_2,Q_3$	0	NC	NC	NC
$P_1,P_2,P_3,K_2,K_4,Q_1,Q_4$	$-V_{dc1}$	+	+	+
$S_2,P_1,P_3,K_2,K_4,Q_1,Q_4$	$-2V_{dc1}$	+	-	+
$P_1,P_2,P_3,K_1,K_3,Q_1,Q_4$	$-V_{dc2}-2V_{dc1}$	+	+	+
$S_1,P_2,P_3,K_1,K_3,Q_1,Q_4$	$-2V_{dc2}-2V_{dc1}$	+	+	-
$S_1,S_2,P_3,K_1,K_3,Q_1,Q_4$	$-3V_{dc2}-2V_{dc1}$	-	-	+
$S_1,S_2,S_3,K_1,K_3,Q_1,Q_4$	$-4V_{dc2}-2V_{dc1}$	-	-	-

III. CASCADED SCMLI USING PROPOSED BASIC UNIT

The proposed cascaded SCMLI topology is presented in Fig. 3. Basically, the topology is obtained by the cascade connection of *m* basic units. This is done to limit the stress voltage across the switches and producing higher output voltage levels using an optimum number of components.

In this cascade structure, all the basic units are symmetrical to each other.Two algorithms for dc sources are mentioned to generate high voltage levels with considerable voltage stress across the switches.

A. First Algorithm: Symmetric

In this algorithm, the value of all the input dc sources is considered to be equal. With this algorithm, each basic unit is symmetrical itself. Each basic unit can generate a maximum output voltage of $6V_{dc}$ and hence produces 13 levels output voltage.

$$V_{11}=V_{12}=V_{13}=...=V_{m1}=V_{m2}=V_{m3}=V_{dc} \quad (1)$$

$$N_{switch}=\frac{7}{6}\left(N_{Level}-1\right) \quad (2)$$

$$N_{cap}=N_{dc}=N_{diode}=\frac{1}{4}\left(N_{Level}-1\right) \quad (3)$$

$$TSV=3\left(N_{Level}-1\right) \quad (4)$$

B. Second Algorithm: Asymmetric

In this algorithm, each basic unit consists of unequal dc voltage sources. Hence, the basic unit is unsymmetrical to itself but all the basic units are symmetrical to each other. On implementing the second algorithm, the basic unitwill produce a maximum voltage of $10V_{dc}$leading to the generation of 21 output voltage levels.

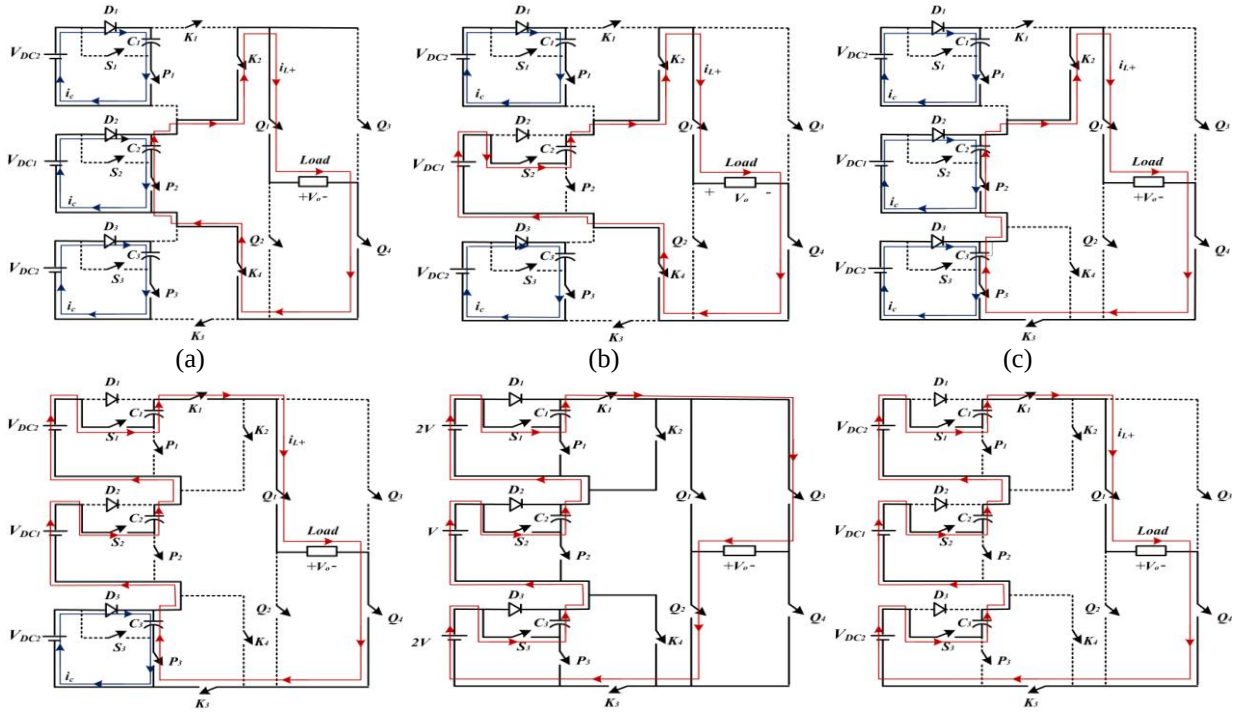

Fig. 2. Current path for different levels; (a) V_{dc1}, (b) $2V_{dc1}$, (c) $(V_{dc1}+ V_{dc2})$, (d) $2V_{dc1}+ 3V_{dc2}$, (e) $-2(V_{dc1}+ 2V_{dc2})$, (f) $2(V_{dc1}+ 2V_{dc2})$

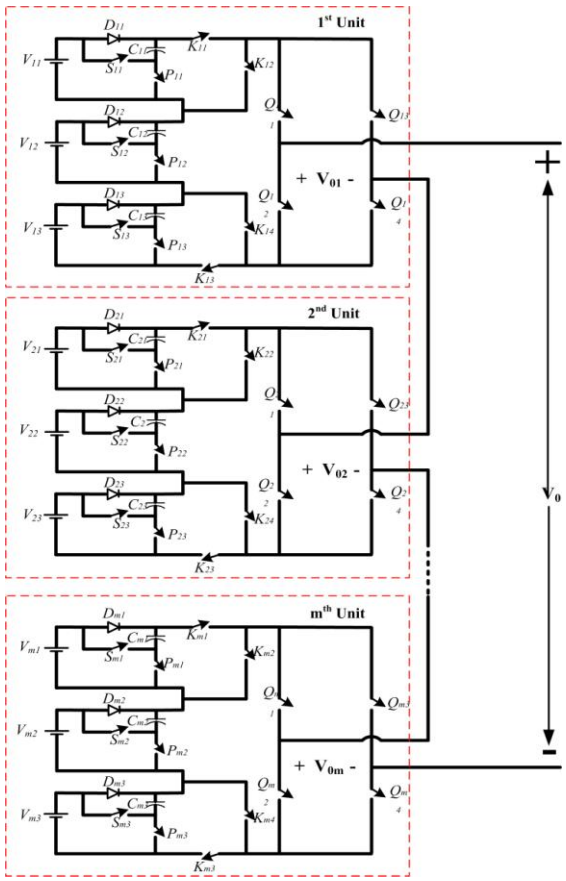

Fig. 3. Proposed Topology

$$V_{11} = V_{13} = ... = V_{m1} = V_{m3} = V_{dc} \quad (5)$$

$$V_{12} = V_{22} = V_{32} = \ldots = V_{m2} = V_{dc} \quad (6)$$

$$N_{switch} = \frac{7}{10}(N_{Level} - 1) \quad (7)$$

$$N_{cap} = N_{dc} = N_{diode} = \frac{3}{20}(N_{Level} - 1) \quad (8)$$

$$TSV = \frac{31}{10}(N_{Level} - 1) \quad (9)$$

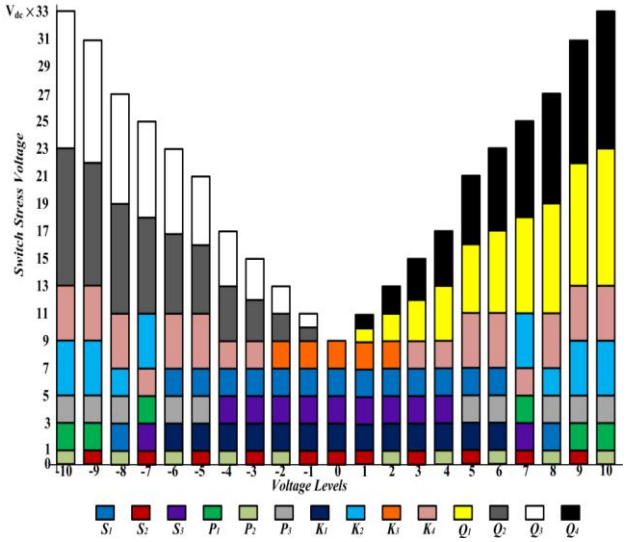

Fig. 4. Switch voltage stress distribution in proposed basic unit for asymmetric dc source algorithm

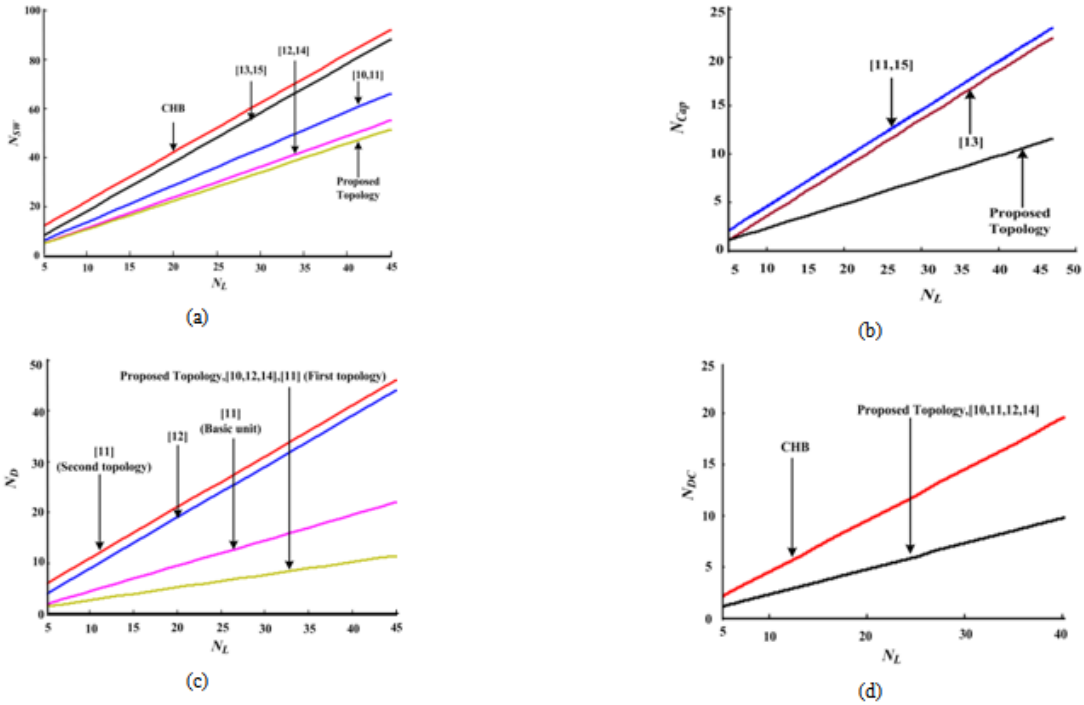

Fig. 5. Variation of required (a) switches, (b) capacitors, (c) diodes and (d) dc supplies versus the generated output voltage level

At the generation of particular voltage levels, the switches which are switched ON exhibit zero voltage across them. However, the switches which remain turned OFF withstand a blocking voltage. Fig. 4 represents the blocking voltage distribution across different switches at particular voltage levels for the proposed asymmetric module.

IV. COMPARISON STUDY

a. Symmetric Comparison

In this section, the comparison study of proposed topologyemploying the first algorithm with CHB, different symmetric SCMLIs**[10-15**] is presented. Fig. 5(a) shows the variation of required switches for all the topologies for producing a specific output voltage level. It is clear that the proposed topology requires minimum power switches in comparison with other topologies for producing a specific output voltage level. The required capacitors and diodes for producing a specific output voltage level for proposed and suggested topologies are shown in Fig. 5(b) and 5(c) respectively. Further, Fig, 5(d) depicts the variation of required dc sources with output voltage levels for different topologies. From these figures, it can be concluded that the proposed topology can produce voltage levels with a lesser number of components as compared to suggested topologies.

b. Asymmetric Comparison

In the comparison study, the proposed topology with the asymmetric algorithm is compared with the SCMLI topologies presented in **[9-10, 13, 15]** and CHB with binary dc source configuration. Table II shows the comparison among proposed topology and the suggested topologies with considering different parameters. It can be observed that the proposed topology required minimum switching devices to produce same output voltage levels.

TABLE II. COMPARISON OF ASYMMETRIC TOPOLOGIES

Variable	CHB(Bin)	[9]	[10]	[13]	[15]	Proposed Topology
N_L	15	7	9	7	9	21
N_{SW}	12	10	12	12	16	14
N_{Cap}	0	3	2	3	3	3
N_D	0	0	2	0	0	3
N_{DC}	3	1	2	1	1	3
N_{VAR}	3	1	1	1	1	3
TSV	28	18	20	12	20	62

V. SIMULATION STUDY

In MATLAB/ SIMULINK, simulation is performed for both 13 level symmetric and 21 level asymmetric proposed SCMLI topology under different loads conditions.

a. Simulation Results of 13 level SCMLI

Simulation of 13 level proposed SCMLI topology is done with the consideration that all the dc sources are equal to 50V. The values for switched capacitors are C_1=C_3=2000µF; C_2=4000µF. Fig. 6(a) shows both the voltage waveform along with current waveform and Fig. 6(b) displays the capacitor voltage under*R-L* load (*R*=100Ω, *L*=25mH). Fig. 6(c) displays the output voltage and corresponding current waveform under inductive load(*L*=125mH)and it can be clearly seen that output current lags the output voltage by 90 degrees. In sudden load change condition i.e. from load 1 (*R*=100Ω, *L*=25mH) to load 2 (*R*=50Ω, *L*=25mH) and the variation of the output voltage and output current is shown in Fig. 6(d). The current waveform changes according to the sudden change in load whereas the output voltage waveform remains unchanged. Fig. 6(e) presents the fast fouriertransform(FFT) analysis of output voltage whereas Fig. 6(f) presents the FFT analysis output current. The voltage Total Harmonic Distortion(THD) and the current THDare 6.45% and 2.72% respectively.

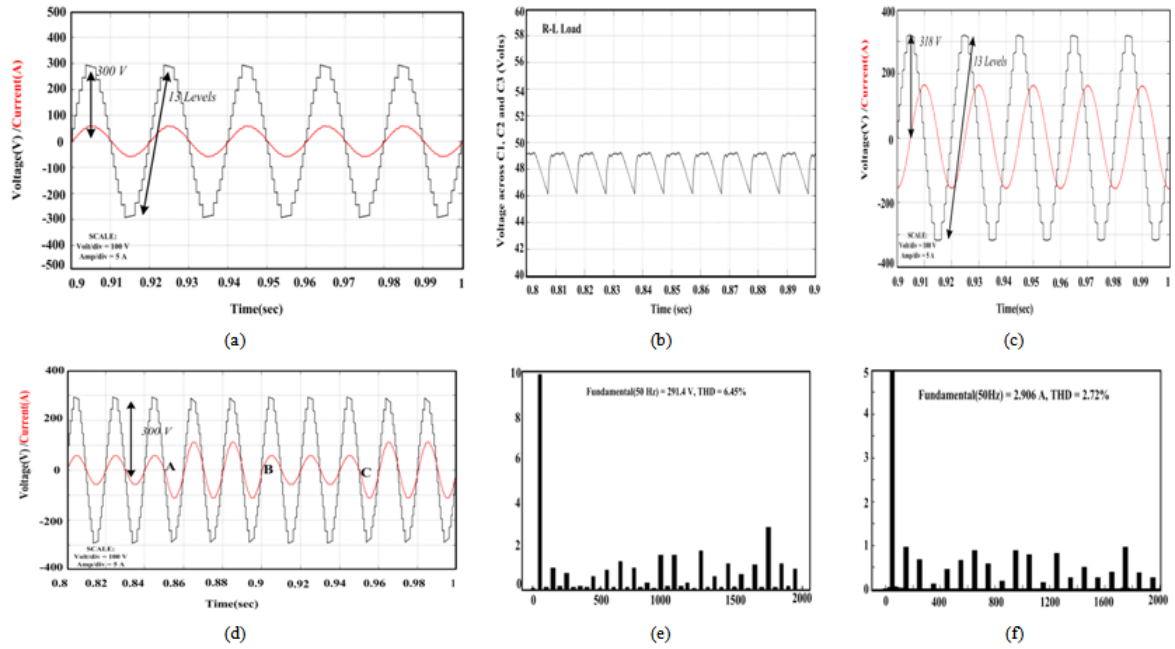

Fig. 6. Simulation results of proposed 13 level SCMLI;(a) Output waveforms under *R-L* load, (b) Capacitor voltage, (c) Output waveforms under *L* load, (d) Output waveforms under sudden load change, (e) Fast Fourier Transform analysis of output voltage, (f) Fast Fourier Transform analysis of output current

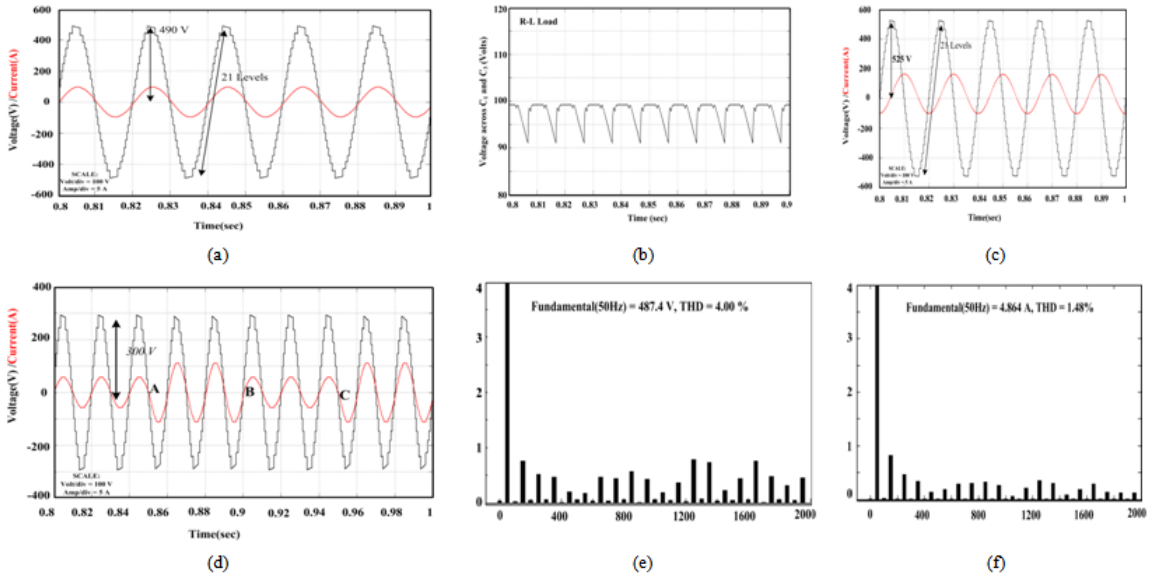

Fig. 7. Simulation results of proposed 21 level SCMLI;(a) Output waveforms under *R-L* load, (b) Capacitor voltage, (c) Output waveforms under *L* load, (d) Output waveforms under sudden load change, (e) Fast Fourier Transform analysis of output voltage, (f) Fast Fourier Transform analysis of output current

b. Simulation Results of 21 level SCMLI

Simulation of 21 level proposed SCMLI topology is done by taking the asymmetric algorithm into consideration. The unequal dc sources employed are 50V and 100 V. The values for switched capacitors are C_1=C_3=2000µF; C_2=4000µF. Fig. 7(a) shows the output voltage waveform along with current waveform under *R-L*load(*R*=100Ω, *L*=25mH). The maximum voltage is found out to be 490 volts. Fig. 7(b) displays the capacitive voltage across $C_1$and C_3under *R-L* load condition. Fig. 7(c) displays the output voltage and current waveform under inductive load(*L*=125mH). Fig. 7(d) displays the voltage and current waveforms under sudden load change conditions. A variable resistance is connected to the load which changes in between 100Ω and 50Ω and the corresponding change in the current waveform is observed. Fig. 7(e) depicts the FFT analysis of the output voltage whereas Fig. 7(f) represents the FFT analysis of output current waveform. The voltage THD and current THD is obtained to be 4.00% and 1.48% respectively.

VI. CONCLUSION

A new cascaded SCMLI topology has been presented in this paper. The proposed basic unit can be represented in both symmetric and asymmetric configuration. In the recommended topology, the basic units are in cascade. The sole objective of this paper is to introduce a novelSCMLI topology which utilizes less number of components to produce a given level. The comparison study of the proposed topology has been performed with the structures presented in the topologies mentioned in this paper. Comparison study indicates that the proposed topology has the least component count. Simulation of both symmetric (13 level SCMLI) and asymmetric (21 level SCMLI) has been carried out. It can be analyzed from the simulations that the proposed topologies can effectively operate in *R-L* load, *L*- load and even in sudden load change condition.

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