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Performance Analysis of NAS-MLI Using FLC with FFT Analysis

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ABSTRACT
A New Asymmetrical Source Multi Level Inverter (NAS-MLI) captivates the need of high power and high voltage outputs. The proposed inverter to reduce Electro Magnetic Interference(EMI), harmonic distortion and high DC link voltage perk up the Multi Level inverters important than the decorous two level inverters. In this paper the comparative analysis of the MLI can be described with different type of controllers and the performance of the inverter has been presented. This topology postulates N number of sources, N*2+4 number of switches in order to produce 4N-1 different levels of outputs. The proposed controller has been developed and simulated using MATLAB/Simulink. The FFT analysis has been obtained to validate the role of the controller.
Keywords: Multilevel inverter, power conversion, SPWM, Asymmetrical source

I. INTRODUCTION

The prevailing Multilevel power conversion methods employ series connection of many semiconductor switches through the clamping diodes which in turn reduces the frequency of the switching and its associated switching losses and issues of the over voltage. Further, the power conversion achieved through the small voltage steps ensures greater power quality and lower voltage stress on the load [1]. The impediment of ML power conversion discusses that the mechanical intricacy rises due to the demand of the greater number of the semiconductor switches and yoked driver gates. It is suggested that the bottom dollar of the ML power conversion can be reduced by using the lower voltage rated switches [2].

The major drawback of the ritual ML power converter is stated as the production of small voltage steps. In spite of the availability of the readymade isolated voltage sources, the necessity of the voltage balance on series capacitors also strengthens the former statement [3]. Even though the supernumerary semiconductor devices address the voltage balancing problem to a certain extent, the outright solution may be yielded by using another ML converter [4]. Since the passion over the ML power conversion drives the researchers for the past two decades, several contemporary converter topologies and modulation methods have been proposed. Cascade converter, NPC converter and flying capacitor inverters are considered as the most innovative groundworks among presented. A cascade 3/2 ML inverter is a combo of two level converters with three level NPC converters [5]. Similarly the fusion of the three level cascade converters with five level NPC converters yields a cascade 5/3 ML inverter [6]. These novel converters are being utilized in FACTs, vehicle propulsion and industrial drives [7-12].

Irrespective of the cost and design issues, ML inverter with multiwinding transformer offers multilevel output. A unique four level inverter gives better response for even number of voltage levels. But it does not acknowledge properly the low or zero output voltage level because of harmonics present at switching frequency. A proposal offers healthy choice of either use of minimum switches or minimum dc voltage. However it bids different series connected voltage sources, more switches and diodes. Though the predominant ML inverters can generate nine output voltage levels with four dc sources, a topology presented by Mondal et.al produces only five output levels [13].

Based on distinct relationship and arrangement between the supplies, an asymmetrical topology is volunteered [14]. In some asymmetrical topologies, the limitation talks about the ratings and performance of the switches and thus restricts the topologies for high voltage products [15]. A novel ML inverter decreases the number of DC sources by inserting many transformer windings which eventually raises the product cost and size [16]. In a new topology, there is a need of more number of switches for the same number of levels. Increasing number of switches again leads to inaccuracy. A deserved topology while matches the value of capacitors to the load current, consequently suffers from balancing of capacitors. If load current increases then the capacitance

should also be vitally increased. This challenge will not be met in all the cases. When modulation index reaches its maxima and minima, in a particular topology, the output voltage is affected by the capacitor voltage and so balancing is needed. This paper manifests a thumbnail of new asymmetrical Multi Level inverter topology. The elucidated topology needs only lesser number of components which exert some of the switches to be operated at the line frequency. This eliminates the functionality of all switches in high frequency and provides lucid and devoted design of inverter [17,18].

In this paper, work is carried out on asymmetrical ML inverter topology which raises the output voltage unlike in symmetrical topologies with Fuzzy Logic Controller (FLC). It adopts the general multilevel schematic and Pulse Width Modulation pulses are taken out from microcontroller to drive the inverter. The same inverter topology can be extended to any number of voltage levels.The enforced simulation work with four DC sources and fifteen levels of outputs is presented. The experimental results for hardware deployment for eight levels of outputs are also put on display.

II. PROPOSED NAS-MLI TOPOLOGY

Figure 1 shows the schematic diagram of proposed topology. This schematic diagram reveals the hardware functionality of the proposed system. In the promoted ML inverter topology, all the power semiconductor switches are not combined to generate bipolar output levels. Instead, the composite of two parts escalate the progress of the topology to newer heights.

Level Generation, the first part accommodates high frequency switches to provoke the output levels.

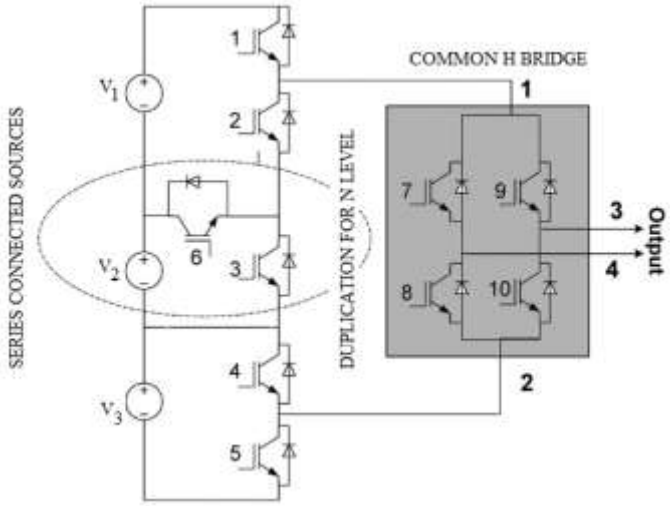

Fig 1: Schematic diagram of topology

Polarity Generation, the later low frequency part employs the full- bridge inverter to generate the required polarity. The left side of the schematic diagram of the topology in figure1 shows series connected asymmetrical DC sources with clamping diodes to generate output voltages at various levels. In symmetrical source method, output voltage is same as the value of the individual source due to the design factor, $V_1=V_2=V_3 =V$, where V is per unit voltage. For example, If $V_1=V_2=V_3 =48V$, then the output voltage will also be 48V.
The asymmetrical source distribution is made in such a way that $V_1=V$ and $V_2=V_3 =2*V$. So it is concluded that in the proposed topology, the output voltage is doubled. For example, $V_1=48V$ and $V_2=V_3 =96V$, it is shown that the output voltage is doubled naturally due to the asymmetry followed in the design. The right side of the schematic diagram of the topology in figure1 shows the common H-Bridge, a full – bridge converter. It transfers the unidirectional output into bi-directional, at the output. Thus the positive or negative polarity of the output signal is decided.

This topology can be further extended to higher voltage levels by duplicating and adding middle stage as required. The topology is thus made suitable for three phase applications. Since isolated and fixed DC supplies are used, the proposed system normally does not address the voltage balancing problems. The proposed topology utilizes fewer numbers of components and less number of carriers for Multi Carrier PWM (MCPWM). This topology requires one modulation signal and so avoids the usage of high frequency switches for the polarity generation part.

As the left part of the recommended topology generates only one polarity, the number of carrier signals needed is reduced into exact half. So, instead of producing fourteen carrier signals, only seven carrier signals are generated. Table 1 interprets the output voltage levels and its corresponding switching sequences. Due to the

felicitous switching sequences, the equivalent output voltage levels are obtained. It is understood that the sum of isolated DC voltage sources stems the final output voltage level.

From the above table1, we can yield a conclusion that the number of output voltage levels is far better in the proposed topology than the conventional one. If the number of isolated DC sources is mentioned as N, then it is effortless to calculate the number of output voltage levels as:

In the existing system, for N sources,

voltage level = 2N+1 levels …1

In proposed system, for N sources,

voltage level = 4N-1 levels …2

Table 1. Number Of Levels, Sources And Switches

No. of Sources N	No. of levels in Existing system 2N+1	No. of levels in Proposed system 4N-1	Sources		Switches	
			E	P	E	P
1	3	3	1	1	6	6
2	5	7	3	2	10	8
3	7	11	5	3	14	10
4	9	15	7	4	18	12
5	11	19	9	5	22	14
6	13	23	11	6	26	16
7	15	27	13	7	30	18
8	17	31	15	8	34	20
9	19	35	17	9	38	22
10	21	39	19	10	42	24

The proposed topology proved that the number of output voltage levels of the proposed system is tremendously increasing for the same number of sources. Thus the equation 1 and 2 can be used for any number of sources. Table 1 discusses the legal relationship between the number of output voltage levels and their correlative number of sources and high frequency switching devices. From the above table 1, we can finalize that the number of switching devices is much lower in the proposed topology than the existing one. From the number of output voltage levels L, we can calculate [L-1]/2, to obtainthe number of sources and the switches as:

No of sources S= 1+ (((L-1)/2)-1)/2 …3

No of switches = S*2+4 …4

From the tables the proposed system gives higher reliability. So the equation 3 and 4 can be used for any number of sources for this asymmetry source multilevel inverter.

III. RESULT AND DISCUSSION

1. Design of Fuzzy Logic Controller

The Fuzzy Logic Controller (FLC) provides an adaptive control for improved system performance [13]. FLC is intended to give solution for controlling the non-linear processes and to handle ambiguous and uncertain situations. The performance of the Controller is developed with MATLAB/Simulink in terms of voltage regulation and variation. The FLC have three stages namely Fuzzification, Rule-Base and Defuzzification. The fuzzy control is developed using input membership functions for error ‘e’ and change in error ‘Δe’ and the output membership function for the duty ratio ‘Δu’ of inverter. The output of the fuzzy control algorithm is the change in PWM Signal [δd (α)]. The PWM Signal d (α), at the α^{th} sampling time, is determined by adding the previous PWM Signal [d (α -1)] to the calculated change in PWM Signal:

$$d(\alpha) = d(\alpha - 1) + \delta d(\alpha) \quad \ldots 5$$

The fuzzy rule variables error ‘e’, change in error ’Δe’ and output ’Δu’ are described by triangular membership functions. The graphical diagram of triangular membership function is shown in figure 2. Seven triangular membership functions are taken for creating the rules. Table 2 present the fuzzy rules. Fuzzy memberships NB,

NM, NS, Z, PS, PM, PB are defined as Negative Big, Negative Medium, Negative Small, Zero, Positive Small, Positive Medium and Positive Big.

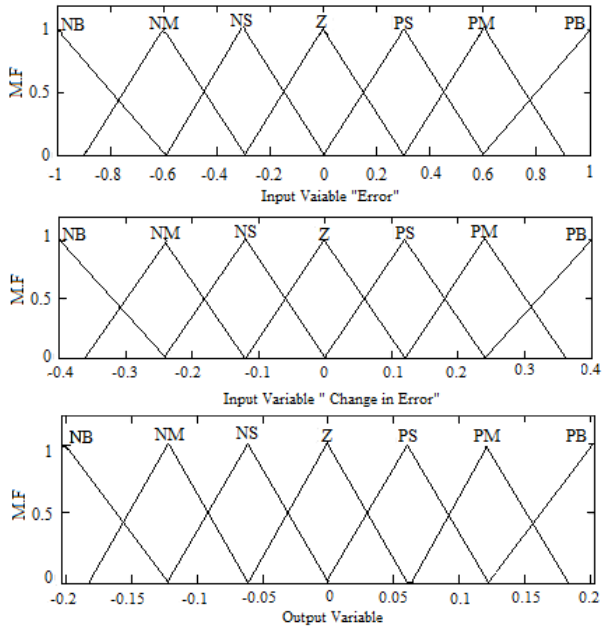

Fig 2: Fuzzy Membership Function Table.2 Fuzzy Rules

	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NS	PS	Z
NM	NB	NM	NM	NS	NS	Z	NS
NS	NB	NM	NB	NS	Z	NS	PS
Z	NB	NS	NS	Z	PS	NM	PB
PS	NS	NS	Z	PS	PB	NM	PB
PM	NS	Z	PS	PB	PB	NM	PB
PB	Z	NS	PS	PB	PB	PB	PB

We have successfully simulated four sources and fifteen output voltage levels Multi Level inverter by using MATLAB Simulink. The hardware is also deployed with two DC sources and seven output levels. The Multi Carrier Pulse Width Modulation MCPWM pulses were generated from the port B of microcontroller. The greater accuracy is achieved by using the digital control over PWM by the micro controller.The designed topology was tested on both resistive and inductive loads and the respective outputs were verified. The maximum output voltage is 325V and the switching frequency of this ML inverter is 5KHZ.
The output of the suggested topology is the result on 50Ω resistive load with Total Harmonic Distortion of 7.13%. The typical outputs are shown in the figure 3 and figure 4.

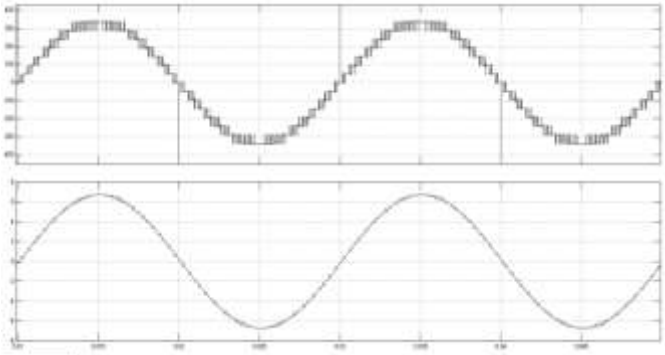

Fig 3: Output on resistive and inductive loads with PWM control

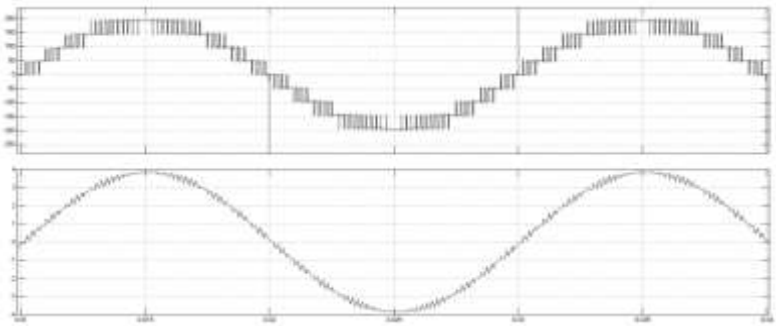

Fig 4: Output on resistive and inductive loads with FLC

The FFT analysis of the proposed NAS-MLI for the output voltage is shown in the figure 5. The Total Harmonic Distortion (THD) is calculated from the inverter side. It's found from the above FFT analysis that the controller tracking performance is good and THD values are less compared to other controller.

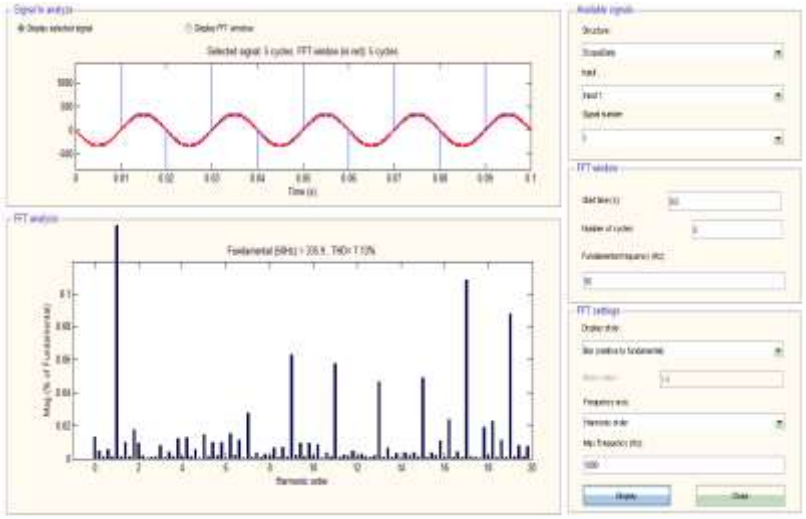

Fig 5 FFT analysis

Table.3 Comparative analysis of transient and steady state performance for different controllers

Controller	Steady state error	Settling Time in Sec.	THD in %
PWM	1	2.36	18.8
FLC	0.04	1	7.13

The performance of the proposed controller response for NAS MLI has been estimated and provided in table 3. It is seen that the FLC based closed loop controllers give the better settling time compared to PWM controller. This ensures that the controller provide the effective feedback. It is concluded from the above table 3 the FLC based controller has improved the transient and dynamic performance of Inverter.

IV. EXPERIMENTAL RESULTS

The proposed model is fabricated and performance is tested. A prototype inverter with controller is operating 300W, 50Hz is designed. The P89V51RD2BN microcontroller is used for generating the driving pulses and IRFP840 MOSFET used as switches in the inverter bridge circuit. MUR4100 diodes are used in the rectifier circuit. The frequency level of the generated PWM is 5 KHz. The open collector opto couplers CYN 17-1 generate the PWM signal from the microcontroller through isolator and IR2110 driver IC. The speed of the motor can be controlled from inverter output. The motor speed is sensed by a digital type pulse sensor GP1L53V. The PWM pulse signal is given to a LM2907 voltage converter IC and feedback signal is given to the microcontroller through an ADC IC ADC0808CCN. Figure 6 shows the hardware setup and figure 7 shows the output of the hardware setup in the Digital Storage Oscilloscope.

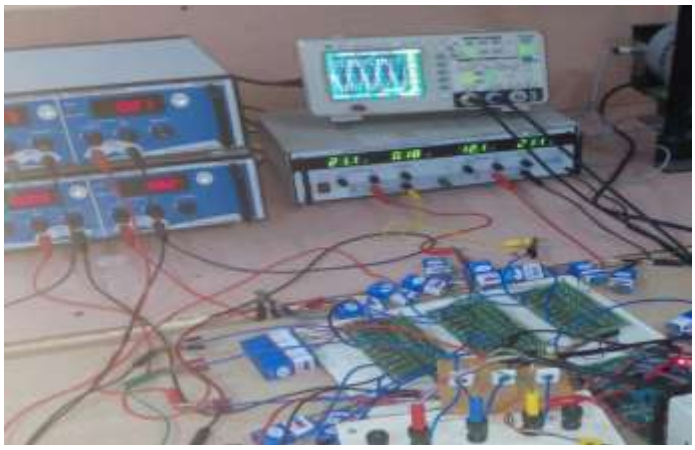

Fig 6: Hardware setup

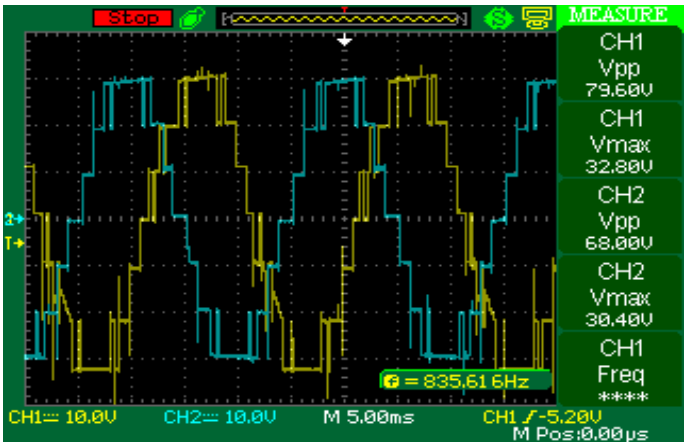

Fig 7: DSO output of the hardware setup

V. CONCLUSION

The proposed controller can be estimated and analyzed with MATLAB/Simulink. It has been found from the analysis that the FLC controller provides better efficiency and high regulation while change in load and supply. The comparison table are presented for transient and dynamic performance of the controllers. It is concluded from the above analysis the proposed FLC controller performs better than other conventional controllers. The harmonics spectrum FFT results obtained from the MATLAB/Simulink. This is to validate, the proposed system was reducing the harmonics in FL controller. The proposed controller provides a good speed tracking without overshoot and less settling time. The proto type model was design and the experimental results are closely agreed with simulation results. All these results arrives a conclusion that the proposed ML inverter topology provides reputable output than the existing system.

REFERENCES

[1]. Ehsan Najafi and Abdul Halim Mohamed Yatim, "Design and implementation of a new Multi level Inverter Topology," IEEE Transactions on Industrial Electronics, vol .59, no.11, November 2012.
[2]. K. Jang-Hwan, S.-K.Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multi level four-leg voltage- source inverter," IEEETrans.Ind.Appl.,vol.44,no.4,pp.1239–1248, Jul./Aug.2008.
[3]. S.Srikanthanand and M.K.Mishra, "DC capacitor voltage equalization in Neutral clamped inverters for DSTATCOM application," IEEE Trans.Ind. Electron.,vol.57, no.8, pp.2768–2775, Aug.2010.
[4]. L.M.Tolbert, F.Z.Peng, and T.G.Habetler, "Multilevel converters for large electric drives," IEEE Trans.Ind. Appl., vol.35, no.1, pp.36–44, Jan./Feb.1999.
[5]. T.L.Skvarenina, "The Power Electronics Handbook. Boca Raton," FL: CRCPress, 2002.
[6]. X.Yun, Y.Zou, X.Liu, and Y.He, "A novel composite cascade multi level converter," in Proc.33rd IEEEIECON, 2007, pp.1799–1804.
[7]. R.H.Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in Conf.Rec.34th IEEEIAS Annu .Meeting, 1999,vol.4,pp.2662–2669.
[8]. E.Najafi and A.H.M.Yatim, "A novel current mode controller for a static compensator utilizing Goertzel algorithm to mitigate voltage sags," Energy Convers.Manage., vol.52, no.4, pp.1999–2008, Apr.2011.
[9]. N.Sekiand H.Uchino, "Converter configurations and switching frequency for a GTO reactive power compensator," IEEE Trans.Ind.Appl., vol.33, no.4, pp.1011–1018, Jul./Aug.1997.

[10]. G.Shahgholiyan, E.Haghjou, and S.Abazari, " Improving the mitigation of voltage flicker by usage of fuzzy control in a distribution static synchronous compensator(DSTATCOM)," MajlesiJ.Elect.Eng., vol.3, no.2, pp.25–35, Jun.2009.
[11]. A.Jidin,N.R.N.Idris, A.H.M.Yatim, T.Sutikno, and M.E.Elbuluk, "An optimized switching strategy for quick dynamic torque control in DTC-hysteresis-based induction machines," IEEE Trans.Ind.Electron., vol.58, no.8, pp.3391–3400, Aug.2011.
[12]. G.M.Martins, J.A.Pomilio, S.Buso, and G.Spiazzi, " Three-phase low-Frequency commutation inverter for renewable energy systems," IEEE Trans.Ind.Electron., vol.53, no.5, pp.1522–1528, Oct.2006.
[13]. S.Daher, J.Schmid, and F.L.M.Antunes, "Multi level inverter topologies for stand-alone PV systems," IEEETrans.Ind.Electron., vol.55, no.7, pp.2703–2712, Jul.2008.
[14]. R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P.N.Enjeti, "Multilevel inverter by cascading industrial VSI," IEEE Trans.Ind.Electron., vol.49, no.4, pp.832–838, Aug.2002.
[15]. D.A.B.Zambra, C.Rech, and J.R.Pinheiro, "A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter," in Proc.Eur.Conf.Power Electron.Appl., 2007, pp.1–10.
[16]. C.Nagarajan and M.Madheswaran, "Experimental Study and steady state stability analysis of CLL-T Series Parallel Resonant Converter with Fuzzy controller using State Space Analysis," Iranian Journal of Electrical & Electronic Engineering, Vol.8 (3), pp.259-267, 2012.
[17]. P. Saravanan, R. Arumugam, M. Senthil Kumaran, "FPGA Based Speed Control of SRM with Optimized Switching Angles by Self Tuning," Circuits and Systems, 7, pp: 1530-1545, 2016.
[18]. Nagarajan C and Madheswaran M - 'Performance Analysis of LCL-T Resonant Converter with Fuzzy/PID Using State Space Analysis'- Springer, Electrical Engineering, Vol.93 (3) , September 2011, pp.167-178.
[19]. Nagarajan C and Madheswaran M – 'Analysis and Implementation of LLC-T Series Parallel Resonant Converter with Fuzzy controller'- International Journal of Engineering Science and Technology (IJEST), Applied Power Electronics and Intelligent Motion Control. Vol.2 (10) , December 2010, pp 35-43.
[20]. Nagarajan.C and Madheswaran.M - 'Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space Techniques'- Taylor & Francis, Electric Power Components and Systems, Vol.39 (8) , May 2011, pp.780-793.
[21]. Nagarajan.C and Madheswaran.M - 'Experimental verification and stability state space analysis of CLL-T Series Parallel Resonant Converter' - Journal of Electrical Engineering, Vol.63 (6) , Dec.2012, pp.365-372
[22]. Murugesan.A and Dr.Jeyabharath.R, "Comparative analysis and Speed control of SR Motor using PID, FLC and ANN Controller with FFT Analysis," Advances in Natural and Applied Sciences, Vol. 10, Issue 17, pp.113-124, 2016.