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High Frequency Performance of Dual Gated Large Area Graphene MOSFET

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ABSTRACT:
This paper presents a detailed study of the high frequency performance of dual gate large area graphene MOSFET. A quasi analytical modeling approach is presented here. To know the high frequency performance of a graphene MOSFET, the drain and output transconductances along with intrinsic gain are calculated here using small signal equivalent model. Finally the cut off frequency of Graphene MOSFET as an important figure of merit is also shown.

KEYWORDS: *Cut-off frequency, Dual gate effects, GFET, Graphene MOSFET, Intrinsic gain, Large area graphene, Self-consistent quantum capacitance.*

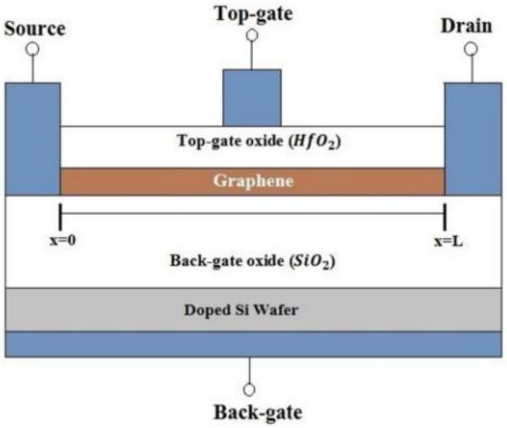
I. INTRODUCTION

Graphene is a single layer of sp^2-bonded carbon atoms that are packed in a honeycomb lattice. It wasn't until the year 2004 that Andre Geim and Konstantin Novoselov managed to produce graphene flakes with a technique called mechanical exfoliation. Geim and Novoselov were awarded the Nobel Prize in Physics in 2010 for their discovery of graphene. It is, therefore, easy to claim that 2010 has been the year of graphene [1]. Graphene offers many of the advantages such as high carrier mobilities up to 2×10^5 $cm^2 V^{-1} s^{-1}$ in substrate supported devices and high saturation velocity [2]−[6]. The novel electronic properties of graphene lead to intense research into possible applications of this material in nano scale devices. The presence of high mobility and high saturation velocity makes graphene very promising for high speed field effect devices as a channel material.

There have been studies on modeling and characterizing of graphene FETs and MOSFETs in different dimensions. However, the progress is at initial stage. In order to fabricate high performance G-MOSFETs, understanding of detailed device modeling and performance evaluations is urgently required. The recent works have been concentrated mostly on the current voltage characteristics of large area graphene MOSFETs using different approaches. However, there have no significant works on high frequency performance although graphene is predicted to highly attracted material for high speed nano-scale devices.

II. MODELING OF GRAPHENE MOSFET

This work is about the modeling of large-area graphene metal-oxide semiconductor field-effect transistors (Graphene MOSFETs). In every FET an electric field is used to change the conductivity of the channel. This electric field is generated by applying a gate voltage to the gate terminal. Thus the name gate can be understood literally. It controls how many electrons can pass the channel. There are two other terminals in all FETs which are essential. These are the source and the drain terminal. Their names refer also to their functions. If a positive drain-source voltage is applied to these terminals, electrons are injected from the source into the channel and collected by the drain. The resulting current is referred to as the drain current. The feature which distinguishes GFETs from other FETs is that the channel is made of graphene.



"**Figure 1.** The cross section of the modeled graphene MOSFET with top- and back-gate" [7].

A simple model of the GFET which is described in this paper is shown in "Figure1". Here the channel is made of large-area single-layer graphene, which has a zero band gap. We have used channel length of 5µm and width of 1µm. It is located on a heavily doped oxidized silicon wafer. This acts as a second gate and is referred to as the back-gate. It is used to control whether the graphene is p- or n-conducting by applying a back-gate voltage. The source terminal is grounded and a drain-source voltage can be applied to the drain terminal. Both contacts between these terminals and the channel are considered to be ohmic. The top-gate is separated from the graphene channel by an insulator and is used to control the charge carrier density and therefore the conductivity in the channel.

2.1. Channel Charge Calculation

Besides modeling the DC behavior of GFETs the goal of this work is also to model the high-frequency characteristics of these devices. This will be done by calculating the elements of the small-signal equivalent circuit. Before we can deal with these elements we need to know how to calculate the channel charge, since this is essential in order to determine the gate-source and gate-drain capacitances. In general the channel charge Q_{ch} can he calculated by subtracting the amount of electrons from the amount of holes and multiplying the result by the elementary charge. This can be written as [2]

$$Q_{ch} = qW \int_0^L (p(x) - n(x))\, dx \tag{1}$$

To obtain Q_{ch}, a simple numerical integration is performed using a trapezoidal approximation. For the model from section 6.1 the calculation of Q_{ch} is a little more tricky since we only know p(V(x)) and n(V(x)). The x dependence of the local hole and electron sheet densities can be translated into a dependence on the local voltage V(x). By using this equation [2]

$$\frac{dx}{dV(x)} = \frac{qW\rho_{real}(V(x))\mu}{I_d} + \frac{\mu}{v_{sat}(V(x))} \tag{2}$$

The overall net charge can be expressed using equation (1) and (2). Thus the necessary equation of Q_{ch} is

$$Q_{ch} = qW \int_0^{V_{ds-int}} [p(V(x)) - n(V(x))] \frac{dx}{dV(x)} dV(x) \tag{3}$$

$$Q_{ch} = \int_0^{V_{ds-int}} [\rho(V(x)) - nV(x)] \left(\frac{qW\rho_{real}(V(x))\mu}{I_d} + \frac{\mu}{v_{sat}(V(x))}\right) dV(x) \tag{4}$$

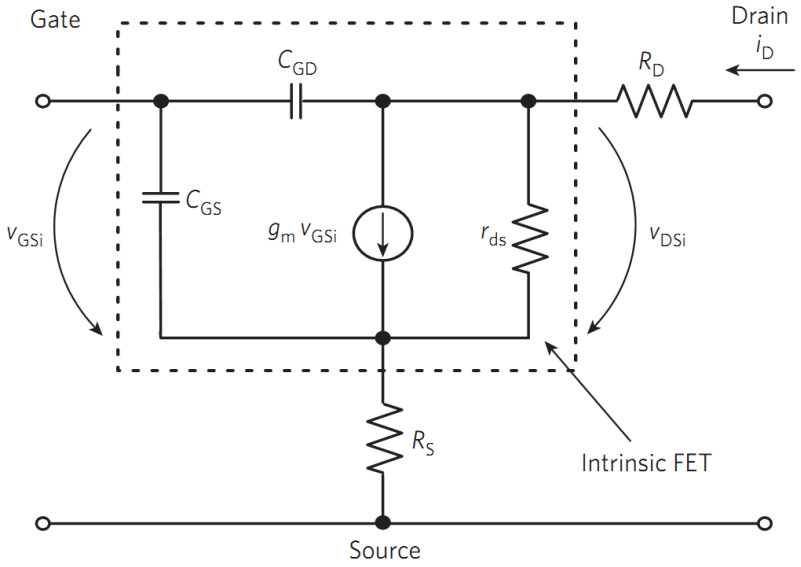
It is important to distinguish between p, n and ρ_{real} in the formula above. If we neglect the minority charge carriers, p(V(x)) — n(V(x)) is equal to ρ_{real} can be expressed as:

$$p(V(x)) - n(V(x)) \cong -(V_{gs-top} - V(x) - V_{gs-top,0}) \frac{\frac{1}{2}C_{ox-top}C_q}{C_{ox-top} + C_{ox-top} + \frac{1}{2}C_q} - (V_{gs-top} - V(x) - V_{gs-top,0}) \frac{\frac{1}{2}C_{ox-back}C_q}{C_{ox-top} + C_{ox-top} + \frac{1}{2}C_q} \quad (5)$$

The integral to determine Q_{ch} is solved numerically. The whole simulation is carried on MATLAB environment.

III. SMALL-SIGNAL EQUIVALENT CIRCUIT

The high-frequency behavior of the transistor can be modeled with a small-signal equivalent circuit [2] as shown in "Figure 2". The intrinsic transistor is described by the transconductance g_m, the drain conductance g_{ds}, the gate-source capacitance C_{gs}, and the gate-drain capacitance C_{gd}. Thereby the whole behavior of the device is described by these four elements: g_m, $g_{ds,}$ C_{gs} and C_{gd}. The reason why this is possible is the following. The high-frequency AC signal is thought to be superimposed onto a DC signal, which defines the DC operating point. If the amplitude of the AC signal is small, the nonlinear transistor characteristics can be linearized around the DC operating point. Thus, all elements of "Figure 2" are explained in the following as mentioned [2].



"Figure 2. The small-signal equivalent circuit of a graphene MOSFET**".**

Here the intrinsic transconductance, g_m, is related to the internal small-signal gate source and drain–source voltages, V_{GSi} and V_{DSi}, whereas the terminal transconductance, g_{mt}, is related to the applied gate–source and drain–source voltages, V_{GS} and V_{DS} [2]."

3.1. Transconductance Calculation

The transconductance calculation is very important to know the radio-frequency characteristics of a graphene MOSFET. They are of two types: intrinsic transconductance and drain transconductance.

3.2. Intrinsic Transconductance, g_m

Transconductance describes the change of the drain current I_d caused by small variations of the internal gate-source voltage $V_{gs\text{-}top\text{-}int}$ at a fixed drain source voltage $V_{ds\text{-}int\text{-}const}$ [2]. In other words, the transconductance is defined as the variation in the drain current I_d caused by a small variation in the top-gate voltage $V_{gs\text{-}top}$ as:

$$g_{m-top} = \left.\frac{dI_d}{dV_{gs-top-int}}\right|_{V_{ds-int}=const} \quad (6)$$

$$g_{m-back} = \left.\frac{dI_d}{dV_{gs-back-int}}\right|_{V_{ds-int}=const} \tag{7}$$

The transconductance due to top-gate voltage ($g_{m\text{-}top}$) and the transconductance due to back-gate voltage ($g_{m\text{-}back}$) can be evaluated using equation (6) and equation (7) clearly. It describes how the output signal (drain current) reacts on changes of the input signal (gate- source-voltage).

3.3. Drain Transonductance of GFET, g_{ds}

The drain-source transconductance g_{ds} describes the resistance of the graphene channel, since it is the inverse of r_d. It is expressed by the variation of the drain current I_d caused by a change of the internal drain-source voltage $V_{ds\text{-}int}$ at a fixed $V_{gs\text{-}top\text{-}int}$.

$$g_{ds-top} = \left.\frac{dI_d}{dV_{ds-int}}\right|_{V_{gs-top-int}=const} \tag{8}$$

$$g_{ds-back} = \left.\frac{dI_d}{dV_{ds-int}}\right|_{V_{gs-back-int}=const} \tag{9}$$

The drain conductance due to fixed value of top-gate voltage ($g_{ds\text{-}top}$) and the drain conductance due to fixed value of back-gate voltage ($g_{ds\text{-}back}$) can be evaluated using equation (8) and (9).

3.4. Intrinsic Capacitance Calculation

The intrinsic capacitance is very necessary to calculate the cut-off frequency and other radio-frequency behaviour of a graphene MOSFET. The mobile channel charge Q_{ch} depends on the top-gate voltage $V_{gs\text{-}top\text{-}int}$, the back-gate voltage $V_{gs\text{-}back\text{-}int}$ and drain-source voltage $V_{ds\text{-}int}$. This dependence is modeled by the gate-source capacitance C_{gs} & the gate-drain capacitance C_{gd} [2].

3.4.1. Gate-Source Capacitance, C_{gs}

The gate-source capacitance Cgs is defined as the variation in the channel charge Q_{ch} caused by a small variation in the top-gate voltage Vgs-top-int with a fixed value of drain-source voltage $V_{ds\text{-}int}$.

$$C_{gs-top} = -\left.\frac{dQ_{ch}}{dV_{gs-top-int}}\right|_{V_{ds-int}=const} \tag{10}$$

$$C_{gs-back} = -\left.\frac{dQ_{ch}}{dV_{gs-back-int}}\right|_{V_{ds-int}=const} \tag{11}$$

The gate-source capacitance due to top-gate voltage ($C_{gs\text{-}top}$) and the gate-source capacitance due to back-gate voltage ($C_{gs\text{-}back}$) can be evaluated using equation (10) and equation (11) clearly.

3.4.2. Gate-Drain Capacitance, C_{gd}

The gate-drain conductance C_{gd} is defined as the variation in the channel charge Q_{ch} caused by a small variation in the drain-source voltage V_{ds-int} with a fixed value of top-gate voltage $V_{gs\text{-}top\text{-}int}$.

$$C_{gd-top} = -\left.\frac{dQ_{ch}}{dV_{ds-int}}\right|_{V_{gs-top-int}=const} \tag{12}$$

$$C_{gd-back} = -\left.\frac{dQ_{ch}}{dV_{ds-\text{int}}}\right|_{V_{gs-back-\text{int}}=const} \tag{13}$$

The gate-drain capacitance due to the fixed value of top-gate voltage ($C_{gd\text{-}top}$) and the gate-drain capacitance due to the fixed value of back-gate voltage ($C_{gd\text{-}back}$) can be evaluated using equation (12) and equation (13) also.

As described earlier, the total amount of charge carriers in the channel is changing with varying $V_{gs\text{-}top\text{-}int}$, $V_{gs\text{-}back\text{-}int}$ and $V_{ds\text{-}int}$. Its dependence is described by two capacitances: the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} as described in the above sections (3.4.1 and 3.4.2).

3.5. Intrinsic Gain Calculation

Finally, we show an example of projection of the intrinsic gain as a figure of merit commonly used in RF/analog applications. In small signal amplifiers, for instance, the transistor is operated in the ON-state and small RF signals that are to be amplified are superimposed onto the DC gate-source voltage [8]. Instead, what is needed to push the limits of many analog/RF figures of merit, for instance the cut-off frequency or the intrinsic gain, is an operation region where high transconductance together with a small output conductance is accomplished. Next, we will give an example on how to use our current-voltage DC model to project an important figure-of-merit (FOM) used in RF applications, namely the intrinsic gain (G).

3.5.1. Intrinsic Top-Gate Gain, G_{top}

The intrinsic top-gate gain G_{top}, which is defined as the ratio of the transconductance (g_{m-top}) to the drain-conductance (g_{ds-top}) expressed as:

$$\text{Intrinsic top-gate gain, } G_{top} = \frac{g_{m-top}}{g_{ds-top}} \tag{14}$$

The top-gate gain (G_{top}) is very important in RF applications as well as cut-off frequency.

3.5.2. Intrinsic Back-Gate Gain, G_{back}

The intrinsic back-gate gain G_{back}, which is defined as the ratio of the transconductance (g_{m-back}) to the drain-conductance ($g_{ds-back}$) expressed as:

$$\text{Intrinsic back-gate gain, } G_{back} = \frac{g_{m-back}}{g_{ds-back}} \tag{15}$$

Both g_m and g_{ds} are small-signal quantities [8]. Here the internal quantities of voltages have to be considered. The intrinsic back-gate gain is more than the intrinsic top-gate gain, as found in our simulation.

3.6. Cut-off Frequency Calculation

Now all elements of the equivalent circuit are known and we are able to calculate the cut-off frequency f_T of the graphene MOSFET [2]. It is related to the short circuit current gain h_{21}, which is the ratio of the small-signal output current to the input current. This ratio is frequency dependent and decreases with increasing frequency. The frequency where this ratio becomes unity is defined at the cutoff frequency f_T, which can be approximated by:

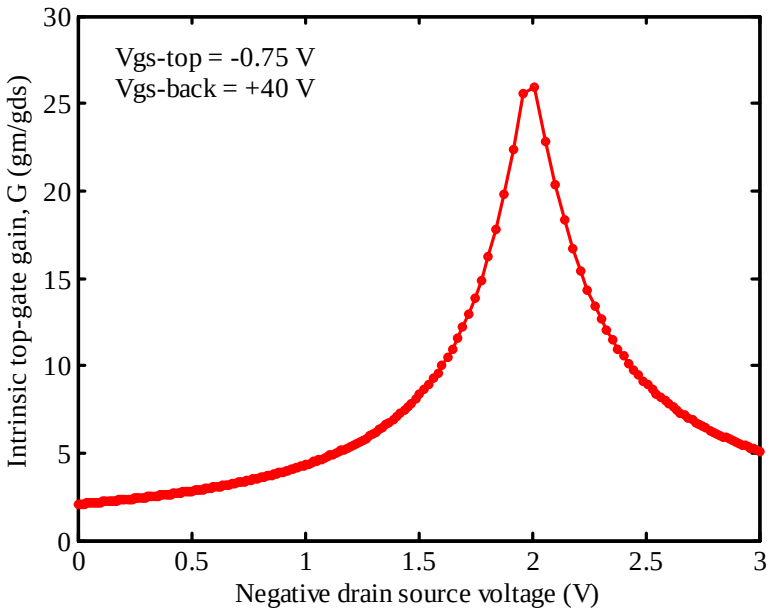
$$f_T = \frac{g_m}{2\pi[(C_{gs}+C_{gd})(1+g_{ds}(R_s+R_d))+C_{gs}g_m(R_s+R_d)]} \tag{16}$$

For large-area GFETs, the output characteristic shows a weak saturation that could be exploited for analog/RF applications. The cut-off frequencies in the THz range are envisioned [8].

IV. RESULTS

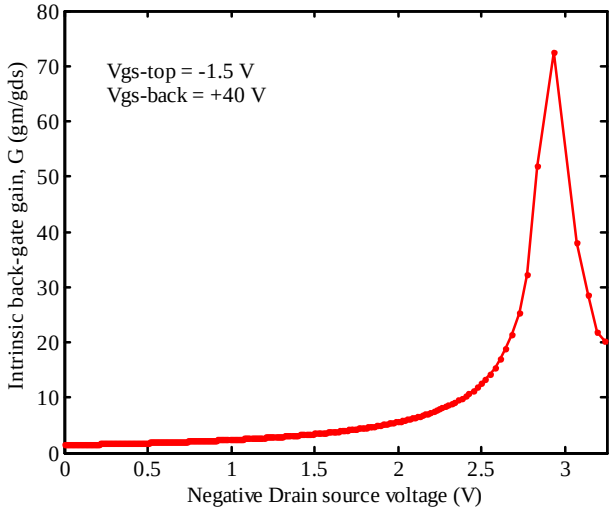
4.1. Intrinsic Top-Gate Gain, G_{top}

"Figure 3" shows that the variation of intrinsic top-gate gain as a function of drain source voltage. Here, the intrinsic peak top-gate gain (G_{top}) is found 25.93 for V_{ds}=—*2.01V* at $V_{gs\text{-}top}$=—*0.75V* and $V_{gs\text{-}back}$=*+40V*. We have found a wide peak at V_{ds} = —*2.01V* when the intrinsic top-gate gain was plotted against the drain to source voltage.



"Figure 3. Intrinsic top-gate gain (G_{top}) as a function of drain source voltage V_{ds} at $V_{gs\text{-}top}$ = —*0.75 V* with $V_{gs\text{-}back}$= *+40V***".**

4.2. Intrinsic Back-Gate Gain, G_{back}



"Figure 4. Intrinsic back-gate gain (G_{back}) as a function of drain source voltage V_{ds} at $V_{gs\text{-}back}$ = *+40V* with $V_{gs\text{-}top}$= —*1.5V***".**

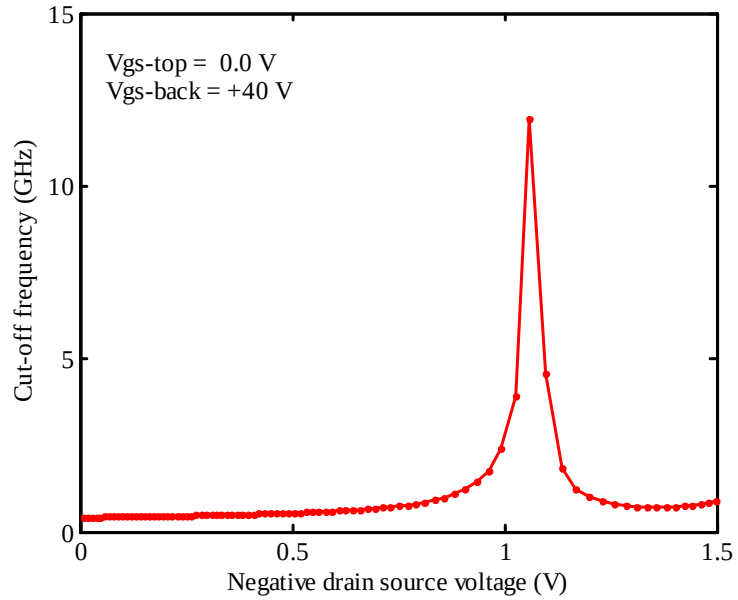
"Figure 4" shows the intrinsic peak back-gate gain (G_{back}) are found 72.38 as a function of drain source voltage *(V_{ds} = —2.934V)* at $V_{gs\text{-}top}$= —1.5V and $V_{gs\text{-}back}$= +40V. We have found a narrow peak at V_{ds} = —2.934V when the intrinsic top-gate gain was plotted against the drain to source voltage. The peak of Intrinsic back-gate gain was found at a higher negative drain-source voltage in comparison with Intrinsic top-gate gain.

4.3. High frequency Performance

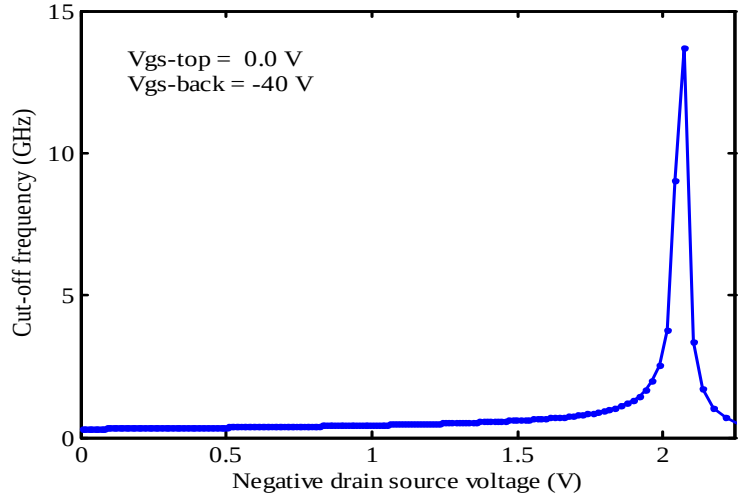
In radio frequency applications the high speed field effect device is desired. In this case of graphene MOSFET the cut-off frequency is also increased in GHz range. We have found a narrow peak of cut-off frequency plotted versus the drain-source voltage that coincides with the inflection point of the output characteristics.

Our simulated peak cut-off frequencies are found 11.96 GHz and 13.69 GHz for back-gate voltage $V_{gs\text{-}back}$ = +40V and - 40V with zero top-gate voltage i.e. $V_{gs\text{-}top}$= 0.0V as shown in "Figure 5" and "Figure 6" respectively.

The resultin high cut-off frequency is very much promising for RF application.



"Figure 5. The cut-off frequency f_T as a function of drain-source voltage V_{ds} with $V_{gs\text{-}top}$ = *0V* and $V_{gs\text{-}back}$ = *+40V."*



"Figure 6. The cut-off frequency f_T as a function of drain-source voltage with $V_{gs\text{-}top}$ = *0V* and $V_{gs\text{-}back}$ = —40V.*"*

V. CONCLUSION

In this paper, the high frequency performance of large area of Graphene MOSFET is studied using quasi-analytical approach. The drain transconductance of the device is computed. The resulting high intrinsic top gate gain ≈ 73 which is promising and important figure of merit for RF devices. In addition, high cut-off frequency of 14GHz is obtained at $V_{ds} = -2.07V$ which is very much promising for high speed nano devices.

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