Implementation of Serial Communication IP for Soc Applications

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Abstract:

The serial communication is very commonly used communication protocol between various peripherals and processor. The current trend is all high speed buses are built with serial communication interface.

The ALTERA's NIOS II soft processor and PowerPC hard processor are widely used in FPGA based CSOC (configurable system on chip) applications. These processers don't have programmable serial links for interfacing with embedded peripherals which are mostly off chip.

In this project it is proposed to implement dynamically configurable serial communication block in Verilog. The developed module shall be interfaced with NIOS II soft processor as a general purpose IO port. The serial interface blocks shall be implemented to handle high data rate serial links and provide parallel interface to the processor.

The Nios II IDE (EDK) shall be used for developing the test application in C programming language. The serial interface blocks which are coded in Verilog shall be synthesized using QUARTUS II EDA tool. The CYCLONE III family FPGA board shall be used for verifying the results on board.

I. INTRODUCTION

In electronic design a semiconductor intellectual property core, IP core, or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. IP cores may be licensed to another party or can be owned and used by a single party alone. The term is derived from the licensing of the patent and source code copyright intellectual property rights that subsist in the design.

IP cores can be used as building blocks within ASIC chip designs or FPGA logic designs It IP cores in the electronic design industry have had a profound impact on the design of systems on a chip. By licensing a design multiple times, IP core licensor spread the cost of development among multiple chip makers. IP cores for standard processors, interfaces, and internal functions have enabled chip makers to put more of their resources into developing the differentiating features of their chips. As a result, chip makers have developed innovations more quickly.

II. Typres of Ip Cores:

The IP core can be described as being for chip design what a library is for computer programming or a discrete integrated circuit component is for printed circuit board design.

A. SOFT CORES:

As the complexity of embedded systems designs increased over time, designing each and every hardware component of the system from scratch soon became far too impractical and expensive for most designers. Therefore, the idea of using pre-designed and pre-tested intellectual property (IP) cores in designs became an attractive alternative. Soft-core processors are microprocessors whose architecture and behavior are fully described using a synthesizable subset of a hardware description language (HDL). They can be synthesized for any Application-Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA) technology; therefore they provide designers with a substantial amount of flexibility.

The use of soft-core processors holds many advantages for the designer of an embedded system. First, soft-core processors are flexible and can be customized for a specific application with relative ease. Second, since soft-core processors are technology independent and can be synthesized for any given target ASIC or FPGA technology, they are therefore more immune to becoming obsolete when compared with circuit or logic level descriptions of a processor.

Finally, since a soft-core processor's architecture and behavior are described at a higher abstraction level using an HDL, it becomes much easier to understand the overall design. This paper presents a survey of the available soft-core processors that are used to design and implement embedded systems using either FPGAs or ASICs.

B. HARD CORES:

Hard cores, by the nature of their low-level representation, offer better predictability of chip performance in terms of timing performance and area.

Analog and mixed-signal logic are generally defined as a lower-level, physical description. Hence, analog IP (SerDes, PLLs, DAC, ADC, etc.) are provided to chip makers in transistor-layout format (such as GDSII.) Digital IP cores are sometimes offered in layout format, as well.

Such cores, whether analog or digital, are called "hard cores" (or hard macros), because the core's application function cannot be meaningfully modified by chip designers. Transistor layouts must obey the target foundry's process design rules, and hence, hard cores delivered for one foundry's process cannot be easily ported to a different process or foundry. Merchant foundry operators (such as IBM,Fujitsu, Samsung, TI, etc.) offer a variety of hard-macro IP functions built for their own foundry process, helping to ensure customer lock-in.

III. Commercial Cores and Tools:

Nios II, Micro Blaze, Pico Blaze and Xtensa are the leading soft-core processors provided by Altera, Xilinx and Ten silica respectively. In this section, we will discuss the important features of each soft-core processor. Nios II by Altera Corporation: Altera Corporation is one of the leading vendors of Programmable Logic Devices (PLDs) and FPGAs.

They offer the Stratix, Stratix II and Cyclone families of FPGAs that are widely used in the design of embedded systems and digital signal processing (DSP) applications. They also provide associated CAD tools such as Quartus II and System-on-Programmable-Chip (SOPC) Builder that allow designers to synthesize, program and debug their designs and build embedded systems on Altera's FPGAs.

The Nios II Processor is their flagship IP soft-core processor and can be instantiated with any embedded system design. This processor is the successor of Altera's original Nios softcore processor and features major improvements focused on the reduction of logic element (LE) consumption on an FPGA and improved performance.

The Nios II Soft-Core Processor is a general purpose Reduced Instruction Set Computer (RISC) processor core and features Harvard memory architecture. This core is widely used with Altera FPGAs and SOPC Builder. This processor features a full 32-bit Instruction Set Architecture (ISA), 32 general-purpose registers, single-instruction 32x32 multiply and divide operations, and dedicated instructions for 64-bitand 128-bit products of multiplication.

The Nios II also has a performance of more than 150 Dhrystone MIPS (DMIPS) on the Stratix family of FPGAs. This soft-core processor comes in three versions: economy, standard and fast core. Each core version modifies the number of pipeline stages; instruction and data cache memories and hardware components for multiply and divide operations. In addition, each core varies in size and performance depending on the features that are selected.

Adding peripherals with the Nios II Processors is done through the Avalon Interface Bus which contains the necessary logic to interface the processor with off-the-shelf IP cores or custom made peripherals. Micro Blaze and Pico Blaze by Xilinx Incorporated: Xilinx Incorporated are the makers of the Spartan and Virtex families of FPGAs. In addition, they also offer soft IP cores that target their FPGAs.

The fundamental components that build up a HW/SW system are a CPU (Central Processing Unit) which processes the information in a system, On-chip RAM (Random Access Memory) to store the instructions for the CPU and a JATG UART (Joint Test Access Group Universal Asynchronous Receiver Transmitter) for communication with the host computer. These components communicate with each other through the system bus, see figure below.

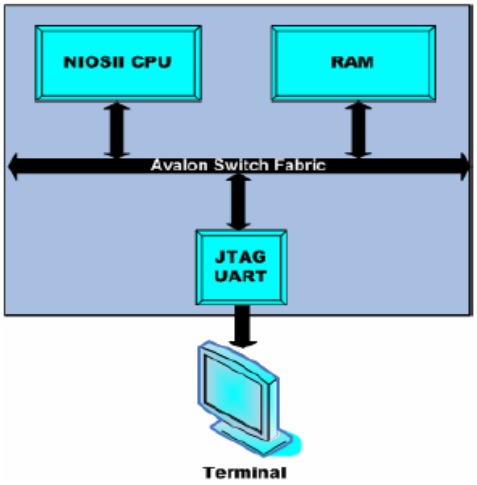

Figure1. system Architecture

The system is generated with the help of SOPC Builder tool. This tool makes easy to specify the system components and their connections and generate a complete system-on programmable- chip (SOPC) in much less time than using traditional, manual integration methods.

IV. Software Development For The System In Niosii Ide:

By this stage the HW structure of the system is complete. To utilize it and verify whether it is working correctly, software has to be created. The programming language that is used is ANSI C. ANSI C (Standard C) is one standardized version of the C programming language. Before the code (software) can be generated and executed, a project has to be built in Nios II IDE("user application project") which in turn needs a system library project ("Hardware Abstraction Layer (HAL) system library project"). The system library is created by Nios II IDE automatically after the user application project is created.

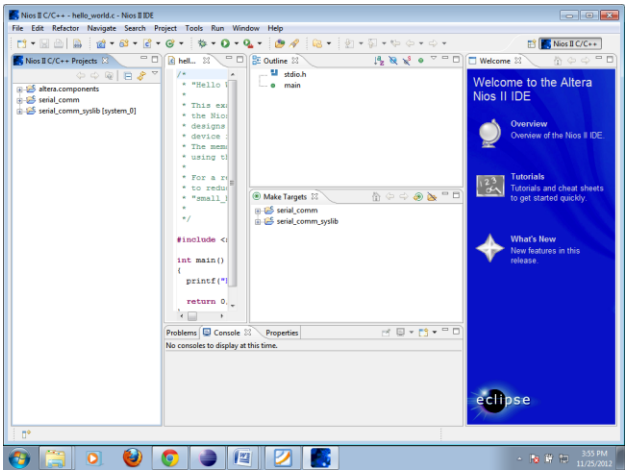

Figure 2. Nios II IDE window.

Flow Summary

Flow Status	Successful - Mon Nov 26 21:58:37 2012
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	esdsd
Top-level Entity Name	serial_commn_top
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	1,600 / 15,408 (10 %)
Total combinational functions	1,509 / 15,408 (10 %)
Dedicated logic registers	832 / 15,408 (5 %)
Total registers	832
Total pins	13 / 347 (4 %)
Total virtual pins	0
Total memory bits	43,008 / 516,096 (8 %)
Embedded Multiplier 9-bit elements	0 / 112 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 3 Performance report

PERFORMANCE REPORT:

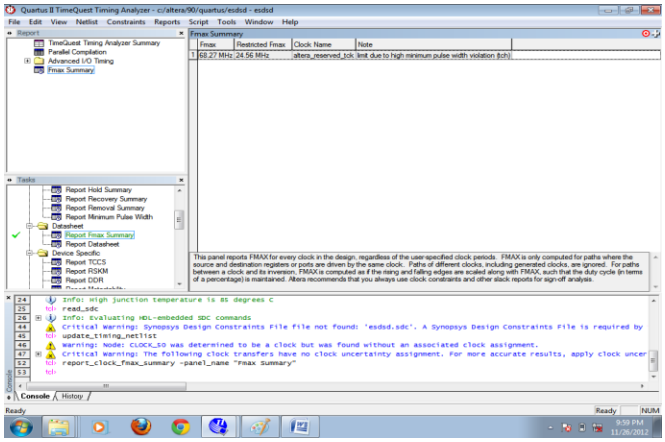

Figure 4. Fmax. Summary report of slow corner.

V. Conclusion

The serial interface blocks are implemented to handle high data rate serial links and provide parallel interface to the processor. The serial interface is interconnected with processor finally through FPGA implementation we verified the functionality. The serial interface blocks which is coded in Verilog is successfully synthesized using QUARTUS II EDA tool. We got the speed rate of around 150MHz clock rate.

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