Implementation of an OFDM FFT Kernel for WiMAX

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Abstract:

In this paper we focus on the OFDM Kernel which refers to the inverse fast Fourier transform and cyclic prefix insertion blocks in the downlink flow and the FFT and cyclic prefix removal blocks in the uplink flow. To support orthogonal frequency-division multiple access (OFDMA) an extension to the OFDM kernel is required that allows each user to be allocated with a portion of the available carriers. This process is referred to as sub channelization. The WiMAX building blocks include bit-level, OFDMA symbol-level, and digital intermediate frequency processing blocks. For bit-level processing, Altera provides symbol mapping/demapping reference designs and support for forward error correction using the Reed- Solomon and Viterbi MegaCore® functions. The OFDMA symbol-level processing blocks include reference designs that demonstrate subchannelization and desubchannelization with cyclic prefix insertion supported by the fast Fourier transform, and inverse fast Fourier transform MegaCore functions. Other OFDMA symbol-level reference designs illustrate ranging, channel estimation, and channel equalization. The digital IF processing blocks include single antenna and multiantenna digital up converter and digital down converter reference designs, and advanced crest-factor reduction and digital predistortion.

Keywords: inverse fast Fourier transform (IFFT), orthogonal frequency-division multiple access (OFDMA), intermediate frequency (IF), forward error correction (FEC), digital up converter (DUC), digital down converter (DDC), crest-factor reduction (CFR), digital predistortion (DPD, WiMAX (Worldwide Interoperability for Microwave Access).

1. Introduction

The Altera® orthogonal frequency division multiplexing (OFDM) kernel can be used to accelerate the development of wireless OFDM transceivers such as those required for the deployment of mobile broadband wireless networks based on the *IEEE 802.16* standard. OFDM is one of the key physical layer components associated with mobile worldwide interoperability for microwave access (WiMAX) and is widely regarded as an enabling technology for future broadband wireless protocols including the 3GPP and 3GPP2 long term evolution standards.

The OFDM kernel has the following key features:

- Support for 128, 512, 1K, and 2K FFT sizes to address variable bandwidths from 1.25 to 20 MHz
- Parameterizable design
- Optimized for efficient use of Cyclone II, Stratix II, and Stratix III device resources

2. Introduction to WiMAX

WiMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard designed to provide 30 to 40 megabit-per-second data rates, with the 2011 update providing up to 1 Gbit/s for fixed stations. WiMAX refers to interoperable implementations of the IEEE 802.16 family of wireless-networks standards ratified by the WiMAX Forum. Similarly, Wi-Fi, refers to interoperable implementations of the IEEE 802.11 Wireless LAN standards certified by the Wi-Fi Alliance. WiMAX Forum certification allows vendors to sell fixed or mobile products as WiMAX certified, thus ensuring a level of interoperability with other certified products, as long as they fit the same profile.

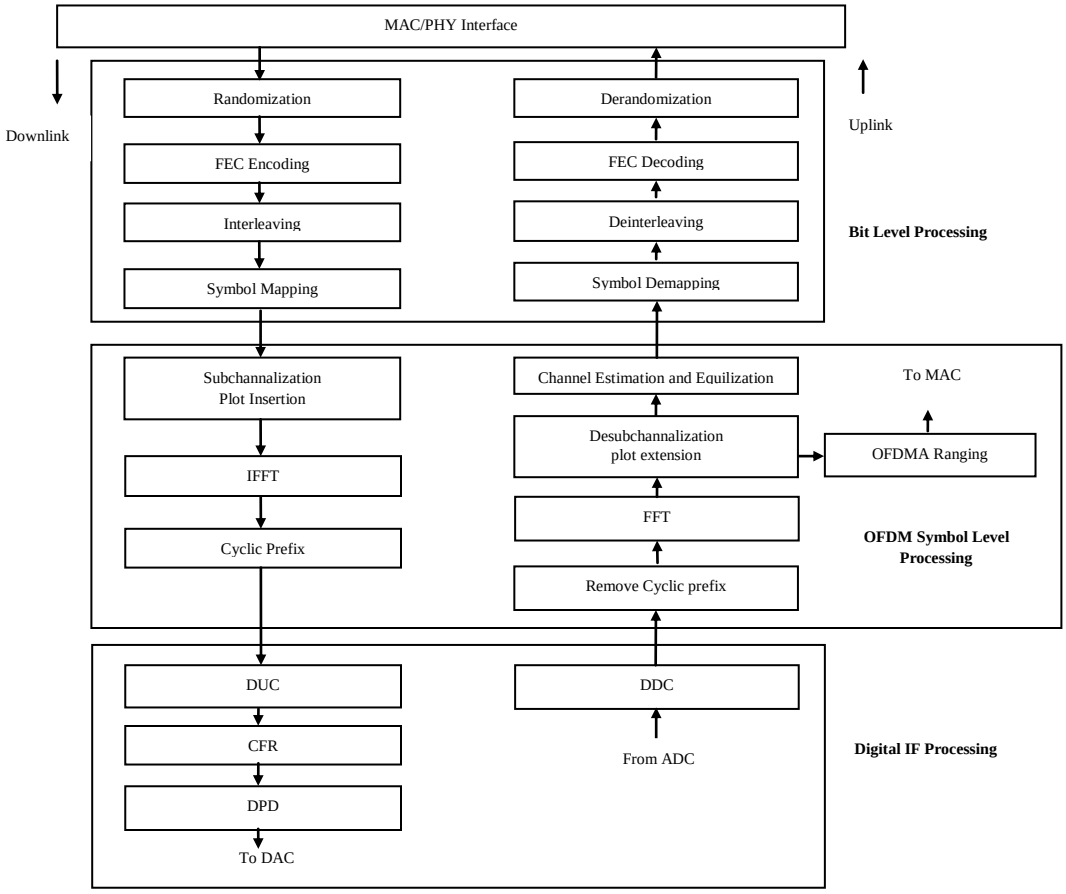


Figure 1. *WiMAX Physical Layer Implementatio*, an overview of the *IEEE 802.16e-2005* scalable orthogonal frequency-division multiple access (OFDMA) physical layer (PHY) for WiMAX basestations.

Altera's WiMAX building blocks include bit-level, OFDMA symbol-level, and digital intermediate frequency (IF) processing blocks. For bit-level processing, Altera provides symbol mapping/demapping reference designs and support for forward error correction using the Reed- Solomon and Viterbi MegaCore® functions. The OFDMA symbol-level processing blocks include reference designs that demonstrate subchannelization and desubchannelization with cyclic prefix insertion supported by the fast Fourier transform, and inverse fast Fourier transform MegaCore functions. Other OFDMA symbol-level reference designs illustrate ranging, channel estimation, and channel equalization. The digital IF processing blocks include single antenna and multiantenna digital up converter and digital down converter reference designs, and advanced crest-factor reduction and digital predistortion.

3. Introduction to OFDM Kernal

The OFDM Kernel refers to the inverse fast Fourier transform (IFFT) and cyclic prefix insertion blocks in the downlink flow and the FFT and cyclic prefix removal blocks in the uplink flow. To support orthogonal frequency-division multiple access (OFDMA) an extension to the OFDM kernel is required that allows each user to be allocated with a portion of the available carriers. This process is referred to as subchannelization. The physical layer is based around OFDM modulation. Data is mapped in the frequency domain onto the available carriers. For this data to be conveyed across a radio channel, it is transformed into the time domain using an inverse fast Fourier transform (IFFT) operation. To provide multipath immunity and tolerance for synchronization errors, a cyclic prefix is added to the time domain representation of the data. Multiple modes are supported to accommodate variable channel bandwidths. This scalable architecture is achieved by using different FFT/IFFT sizes. This reference design supports transform sizes of 128, 512, 1,024, and 2,048.

4. Implementing OFDM Kernal for WiMAX

FPGAs are well suited to FFT and IFFT processing because they are capable of high speed complex multiplications. DSP devices typically have up to eight dedicated multipliers, whereas the Stratix III EP3SE110 FPGA has 112 DSP blocks that offer a throughput of nearly 500 GMACs and can support up to 896 18x18 multipliers, which is an order of magnitude higher than current DSP devices.

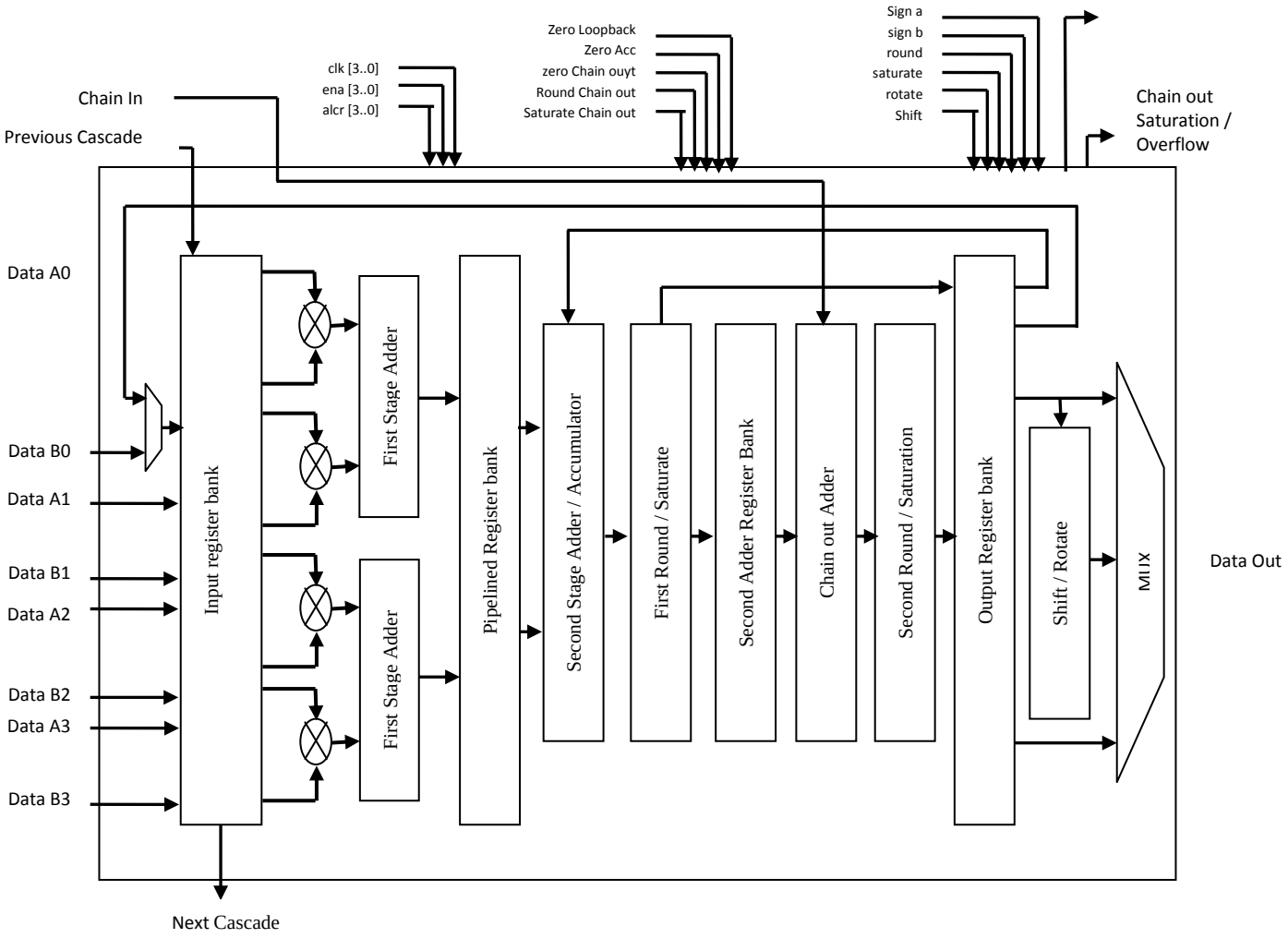


Figure2. Embedded DSP Blocks Architecture in Stratix III Devices

Such a massive difference in signal processing capability between FPGAs and DSP devices is further accentuated when dealing with basestations that employ advanced, multiple antenna techniques such as space time codes (STC), beam forming, and multiple-input multiple-output (MIMO) schemes. The combination of OFDMA and MIMO is widely regarded as a key enabler of higher data rates in current and future WiMAX and 3GPP long term evolution (LTE) wireless systems. When multiple transmit and receive antennas are employed at a basestation, the OFDMA symbol processing functions have to be implemented for each antenna stream separately before MIMO decoding is performed. The symbol-level complexity grows linearly with the number of antennas implemented on DSPs that perform serial operations. For example, for two transmit and two receive antennas the FFT and IFFT functions for WiMAX take up approximately 60% of a 1-GHz DSP core when the transform size is 2,048 points. In contrast, a multiple antenna-based implementation scales very efficiently when implemented with FPGAs. Using Altera devices, we can exploit parallel processing and time-multiplexing between the data from multiple antennas. The same 2×2 antenna FFT/IFFT configuration uses less than 10% of a Stratix II 2S60 device.

5. Functional description of OFDM kernal for WiMAX

Altera provides the reference design as clear text VHDL. The reference design also demonstrates the use of the FFT MegaCore function. To accelerate integration with Altera intellectual property (IP) or other subsystems, the interfaces support the Altera Avalon® Streaming (Avalon-ST) interface specification. Altera has verified the RTL behavior against a fixed point model of the algorithms. The reference design includes RTL testbenches that stimulate the designs using golden reference data from the fixed point model and check for correct functionality. The OFDM kernel handles the FFT operations and cyclic prefix addition and removal. The FFT size is a parameter that we must specify at synthesis time, but we can change the guard interval at run time.

Downlink Transmit

The downlink OFDM kernel module performs an inverse Fourier transform of the frequency domain input data and adds a cyclic prefix to the resulting time domain data. The cyclic prefix addition block contains a controller that buffers the output packets from the FFT, and adds the appropriate proportion of the end of the output packet to the beginning of the output packet. As this requires a fairly significant memory resource, the hardware architecture has been designed so that the embedded memory may be shared with the uplink OFDM kernel if the modem is operating in time division duplex (TDD) mode.

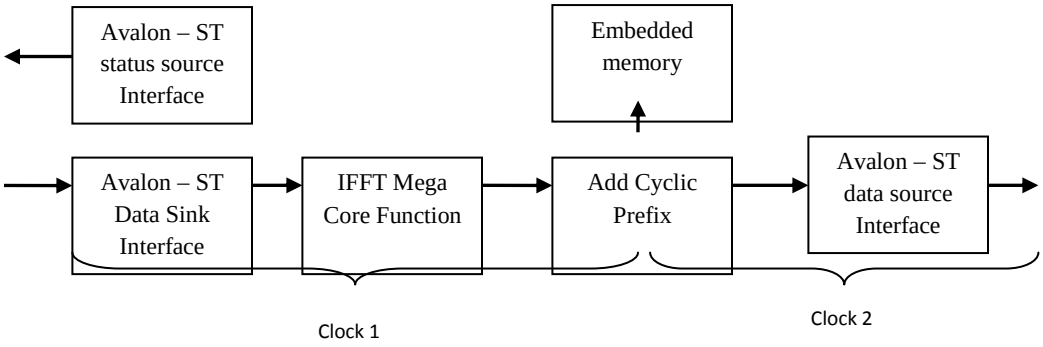


Figure 3 shows a block diagram of the downlink OFDM kernel.

Interface Specifications

The block has two clock domains. In addition, there are two reset ports; one for each clock domain. The reset ports are active low. Figure 4 shows the downlink OFDM kernel interfaces.

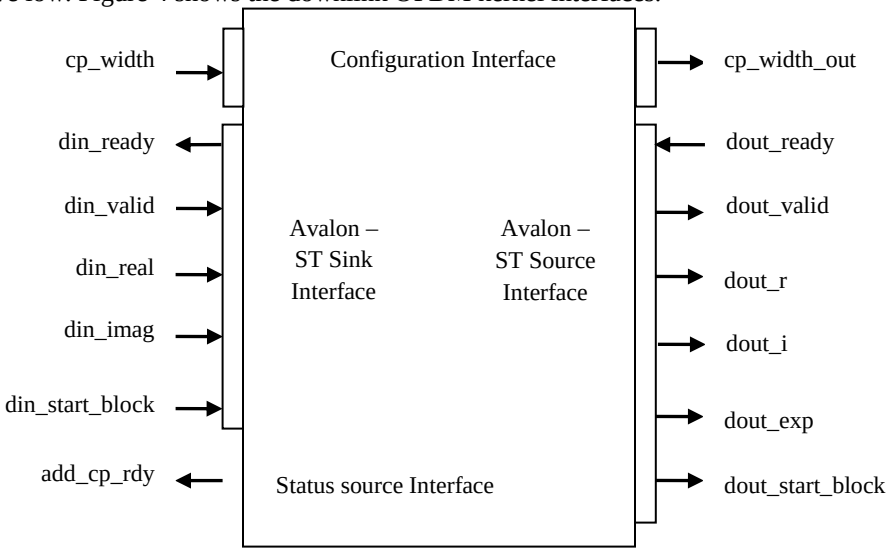


Figure4. Downlink OFDM Kernel Interfaces

The input interface has the following features:

- Avalon-ST data sink and status source
- Ready signal latency of one cycle—the earliest time valid data may be presented to the block after ready has been signaled is one clock cycle

The output interface has the following features:

- Avalon-ST data source
- Ready signal latency of four cycles—the block responds to new data or stops delivering data four cycles after an event on the ready signal
- Support for back pressure and Dynamically changeable cyclic prefix

Uplink Receive

The uplink OFDM kernel module performs an FFT of the time domain input data and removes the cyclic prefix. The Avalon-ST start of packet pulse should specify the start of the cyclic prefix. The remove cyclic prefix block ignores the data during the cyclic prefix and writes the remaining samples to the FFT input buffer.

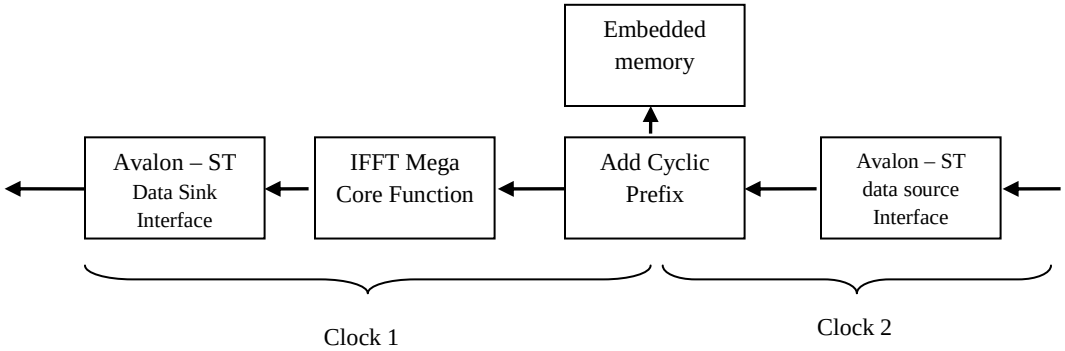


Figure5. Uplink OFDM Kernel Block Diagram

Because the channel characteristics can change, it is possible that the start of the packet pulse is not always after the start of the cyclic prefix time. The hardware has been designed to deal with this scenario but with the constraints that the variation of the pulse must be within the cyclic prefix time and that the start pulse will not be before the preceding symbol has been fully clocked in.

Uplink Interface Specifications

The block has two clock domains. In addition, there are two reset ports; one for each clock domain. The reset ports are active low.

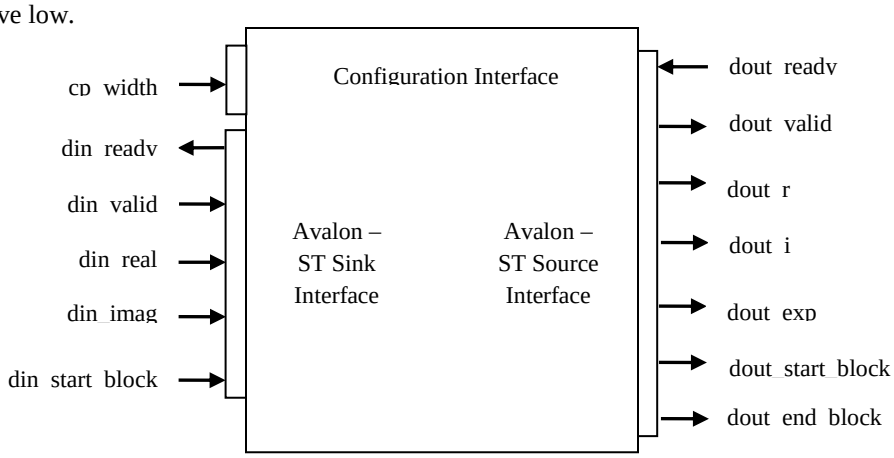


Figure6. Uplink OFDM Kernel Interfaces

The input interface has the following features:

- Avalon-ST data sink
- Ready signal latency of one cycle
- Does not apply back pressure since data is continuous from RF card

The output interface has the following features:

- Avalon-ST data source
- Ready signal latency of one cycle
- Does not accept back pressure from downstream sink
- Dynamically changeable cyclic prefix

FFT MegaCore Function

The FFT MegaCore function is capable of performing both the forward and inverse transform. The hardware architecture is chosen to minimize the resource usage and has the following parameters:

- Burst mode
- Single output engine
- Single instance of engine
- 16-bit internal and data input/output precision widths

In addition, design implements two clock domains so that it is possible to exploit time sharing and minimize resource utilization in the FFT MegaCore function by running Clock 1 faster than Clock 2. The FFT MegaCore function generates block floating point output data and the output dynamic range is maximized for the given input and output data widths.

Clock Requirements

The clocking requirements are as follows:

- The two clock domains must be synchronous
- The minimum Clock 2 frequency is the data sampling frequency given in Table 1. This would lead to a constant output from the FFT MegaCore function

FFT Points	Bandwidth (MHz)	Clock 2 (MHz)
128	1.25	1.429
256	2.5	2.857
512	5	5.714
1,024	10	11.429
2,048	20	22.857

Table 1. Minimum Clock 2 Rate

- The Clock 2 frequency may equal or exceed the Clock 1 frequency
- The Clock 1 requirements are dictated by the FFT MegaCore function and are summarized in Table 2

FFT Points	Required data rate (MHz)	FFT throughput (Cycles/ N block)	Clock 1 minimum Speed (MHz)
128	1.429	858	9.579
256	2.857	1,626	18.146
512	5.714	3,693	41.214
1,024	11.429	7,277	81.220
2,048	22.857	16,512	184.285

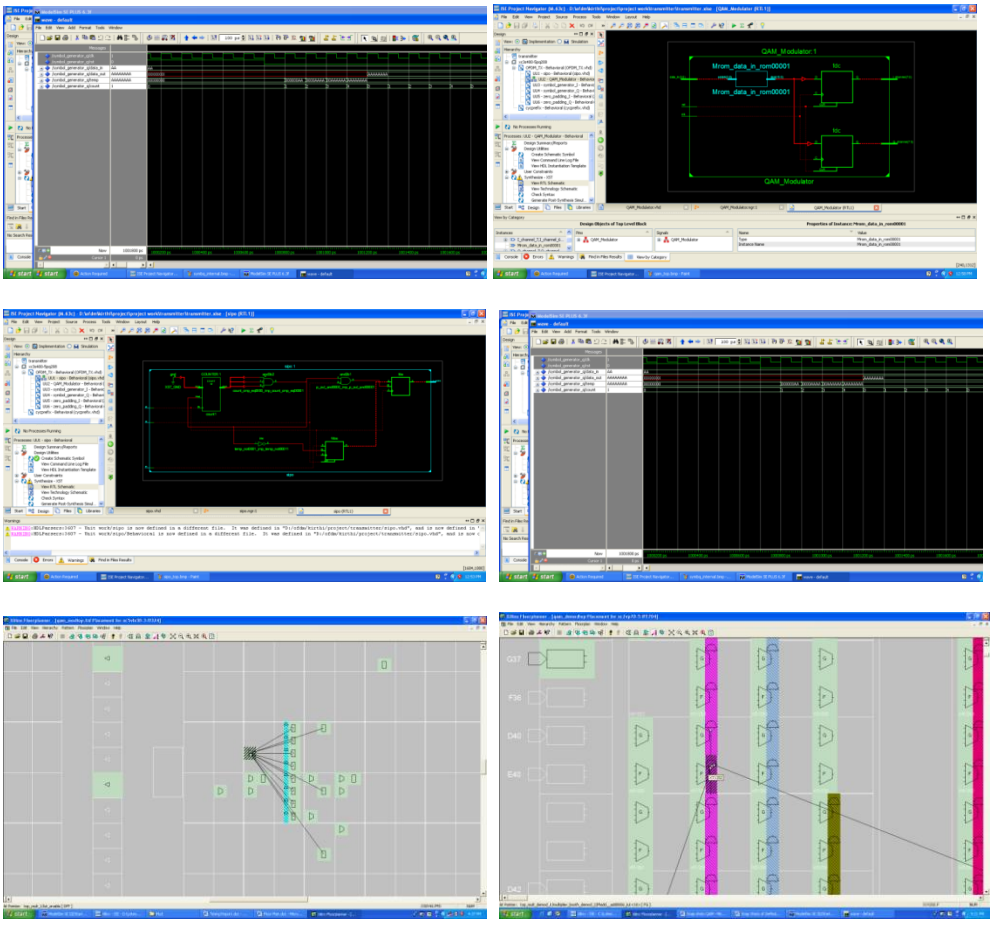
Table 2. Clock 1 Requirements

- Table 2 ignores the cyclic prefix effect, which reduces the Clock 1 speed requirement slightly
- The Clock 1 minimum speed = throughput/*N* × data rate

6. Conclusion

This application note has outlined the advantages of using Altera FPGAs for implementing OFDM systems such as an IEEE 802.16e deployment. A flexible, high-throughput DSP platform needs an FPGA-based implementation platform. In addition, this reference design demonstrates the implementation of a key function that may be exploited to facilitate rapid system deployment.

7. Results



Symbol generator simulation output of an OFDM kernel for WiMAX as obtained in Model Sim®

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