Comparative Study and implementation Mixed Level&Mixed Signal Simulation using PSpice and VHDL

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Abstract:
PSpice CMOS & Logic Gates package that is used to analyze and predict the performance of analog and mixed signal circuits. It is very popular especially among Printed Circuit Board (PCB) engineers to verify board level designs. However, PSpice A/D currently lacks the ability to simulate analog components connected to digital circuits that are modeled using Hardware Descriptive Languages (HDLs), such as VHDL and Verilog HDL. Simulation of HDL models in PSpice A/D is necessary to verify mixed signal PCBs where programmable logic devices like Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) are connected to discrete analog components. More than 60% of the PCBs that are designed today contain at least one FPGA or CPLD. This paper investigates the possibility of simulating VHDL models in PSpice A/D and also coming future implemented solar cell on various sectors in the trainer kit . A new design methodology and the necessary tools to achieve this goal are presented. The new design methodology will help engineers verify a complete mixed signal design at the board level. This reduces design failures and hence increases reliability. It also reduces the overall time to market. A mixed signal design of softwares,Combinational circuits, analog circuits and Electronic Components are used in the DC motor where efficiency economy and performance are essential .this flexible ,inexpensive circuit eliminates costly PWM devices and complex floating upper rail drives, while delivering efficient motor control and Protection. The application is implemented by following the proposed design methodology.

Keyword: A/D, CMOS, CPLD,D/A, FPGA, SCHEMATIC ,PSPICE ,VHDL

1. Introduction

Over the past few decades, PCBs have brought significant change and advancement to the electronics industry. The overall cost, shape and size of many modern day electronic equipments are dependent on thesize and complexity of the PCB that is utilized. A complex board can contain printed circuitry on both its sides or in many layers, which allows great circuit density and compactness. With the increase in the complexity and reduced time to market, Computer Aided Design (CAD) tools are required to design PCBs,and the need for the CAD tool to support and automate complex design tasks have always remained persistent

The Complexity of the design, necessity to increase design efficiency and to reduce time to design, drives the circuit design methodology and the choice of Electronic Design Automation (EDA) tools. Design methodologies are typically classified into Top down design methodology enables designers to refine an abstract idea progressively as the design process continues. The design process could begin with a very high level behavioral definition of the system and then it can get down to finer details with Register Transfer Level (RTL) and gate level descriptions, as the design progresses. This methodology is more popular with digital circuit designs with the advent of HDLs, Programmable Logic Devices (PLDs) and logic synthesis tools . Traditional or bottom up design methodology allows designers to pick components individually (from a standard set of libraries) and build the design by connecting them appropriately. This methodology is popular in the PCB design flow .Large and complex systems are usually broken into smaller units. These units can be designed using different methodologies. Due to difference in levels of design abstraction, different EDA tools are required to work with different design methodologies. This curtails the ability to verify the functionality of the whole system, which is a potential cause for design failures. Moreover a majority of today's designs are mixed signal circuits, circuits containing different signal domains (eg. analog and digital). A typical example of such a design would be a PCB which has PLDs along with other discrete analog components. In awake of such scenarios, rises a need to have EDA tools that are capable of simulating mixed signal designs as well as designs designed using different methodologies. Such simulations are called mixed level and mixed signal simulation. PSpice A/D, which is very popular among PCB designer, supports mixed signal simulation using traditional design methodology. It however lacks the ability to simulate digital designs modeled using HDLs such as VHDL, Verilog etc.. By enabling simulation of VHDL models in PSpice A/D it is possible to realize a mixed level simulator from a mixed signal simulator. This integrates traditional

designing methodology with top down design methodology and hence helps in verifying the functionality of the whole system and identifying problems much earlier in the design cycles. This paper proposes a new design methodology that will allow simulation of synthesizable VHDL models in PSpice A/D along with discrete analog circuits and provides a low-cost solution for simulating mixed signal designs containing VHDL models for FPGAs and/or CPLDs. However the simulation time of such designs will be directly proportional to the number of gates produced after synthesizing the RTL VHDL.

2. Proposed Design Methodology

A design methodology to achieve total system verification at a board level is presented in figure 1. The complex mixed signal design is divided into two sections, namely analog and digital. While the analog circuits are designed by following the traditional design methodology using PSpice A/D schematic editor, the digital portion in VHDL follows the top down design methodology. Finally, the interfacing software (See Section 3B) abridges the two design methodologies by enabling functional verification of the mixed signal design in PSpice A/D. Verification at PCB level requires the simulation medium to support multiple signal domains (analog and digital) along with different design methodologies (traditional/top down). PSpice A/D is a verification software that already supports mixed signal domains. However, it has limitations in design abstraction levels and most of its digital constructs are available only at gate level. The ability to simulate VHDL models in PSpice will allow verification of designs that are defined using different methodologies. To achieve this goal, the proposed methodology employs a logic synthesis tool (Synplify®), which translates any (RTL) VHDL design into it's equivalent gate level (VHDL) description. Logic synthesis retains the essence and rapidness of top down design methodology and allows engineers to describe designs in a high level abstract and be less concerned about the actual implementation A synthesized VHDL description (gate level netlist) represents the digital system in terms of logic gates and the synthesis tool, Synplify generates a gate level VHDL description that is specific to a technology(FPGA, CPLDs architectures from vendors like Xilinx, Altera, Actel etc.) that was chosen during the logic synthesis process. In order to simulate this gate level VHDL description in PSpice A/D, the resulting netlist needs to be in a format that is understood by the PSpice simulation engine. In other words, the gate level VHDL netlist requires to be translated into a PSpice subcircuit definition. Besides this requirement, simulation of technology-specific gate level VHDL description in PSpice also requires the need for appropriate digital device models within PSpice model libraries. The choice of the technology during logic synthesis determines the ease of translation and the ability to avail or create digital device models in PSpice. Typically, CPLD architectures are relatively simple when compared with FPGAs. CPLDs implement digital circuitry in terms of combinatorial and sequential logic functions. Considering these factors the digital logic described in VHDL is synthesized by targeting at Lattice MACH 111 family of CPLDs. The gate level VHDL description generated by Synplify (synthesis tool) can be translated into a PSpice subcircuit definition and it also contains digital devices that are either currently available or that can be modeled in PSpice A/D. The design flow in this proposed methodology is as follows .The digital logic is described in VHDL and simulated to verify its functionality (top down design methodology)

The RTL VHDL code is synthesized in Synplify using Lattice MACH 111 as the target technology. The gate level VHDL description (after synthesis) is functionally verified for logical equivalency

The gate level netlist is now converted into a PSpice circuit file using the interfacing software which was developed as a part of this research.

The Circuit file is converted into a schematic symbol which can be placed on Cadence OrCAD® Capture (schematic editor) along with other analog components and the complete mixed signal design is verified by simulating in PSpice A/D
The translation of the gate level VHDL netlist into its equivalent PSpice circuit file requires
1. A library of PSpice models for Lattice MACH 111 components.

2. Interfacing software that will utilize components from this library and create a PSpice subcircuit file from the gate level VHDL netlist.

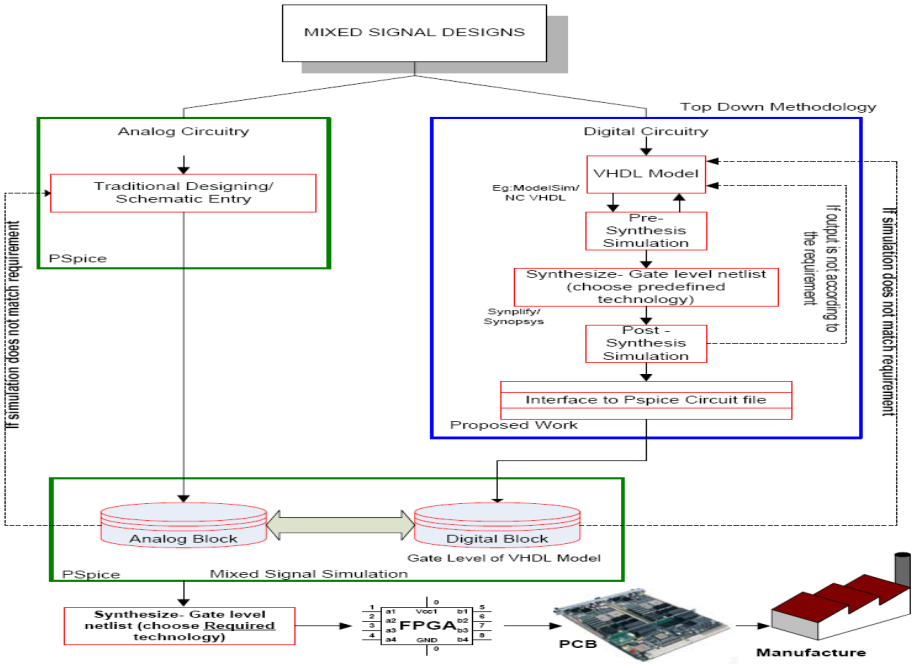


Fig. 1. Proposed design methodology

A. PSpice library of Lattice devices

The gate level VHDL netlist generated by Synplify (synthesis tool) contains components specific to Lattice MACH 111 technology. The following set of combinational and sequential logic elements from the MACH
111 family are utilized by the interfacing software during the translation process.

Combinational logic elements

1) IBUF - Input Buffer
2) OBUF - Output Buffer
3) INV - Logic inverter
4) OR2 - 2 Input logic OR
5) XOR2 - 2 Input logic XOR
6) AND2 - 2 Input logic AND

Sequential logic elements

1) MACHDFF - Reset predominant D flip flop with low preset and reset
2) DFFRH - Reset predominant D Flip flop with preset remaining HIGH all times
3) DFFSH - Reset predominant D Flip flop with reset remaining HIGH all times
4) DFF - Reset predominant D Flip flop The functional behavior of these logic elements are modeled in

PSpice and a library of device models is created for every component that is present in the gate level VHDL netlist.

B. Interfacing software

In the previous section, the creation of PSpice models for Lattice MACH digital devices was discussed. Next, the gate level VHDL netlist needs to be translated into a PSpice subcircuit file. A software program was developed to perform this task. This program will be the interface between the gate level VHDL description and PSpice A/D. Figure 2 presents a flow chart to translate gate level VHDL description into a
PSpice circuit file. The gate level VHDL netlist follows a typical pattern of structured VHDL logic description (Component declaration and definition followed by the main entity and architecture). For every
component defined in the gate level VHDL netlist, there exists an equivalent PSpice model. The interfacing program reads through the gate level VHDL netlist, identifies a Lattice MACH device and replaces it with its equivalent PSpice model in the subcircuit file which it writes simultaneously. The following procedure is followed by the interfacing software

1. Parse through the gate level VHDL netlist and skip until the Main Entity within the file is reached.
2. Within the Main Entity, extract the name of the inputs and outputs. If the inputs/outputs are declared as a BUS, elaborate the bus entries and assign individual net names for each one of the bus entries. PSpice digital device modeling language does not permit BUS declaration.
3. Using the input and output names obtained, define the subcircuit header in the PSpice circuit file by following the PSpice modeling language syntax.
4. Continue to parse the VHDL file and skip until the Main Architecture of the entity is reached.
5. Within the Main Architecture, skip the section where internal signal and component names are declared.
6. Scan the architectural definition and identify the Lattice MACH device that is being "port - mapped"
7. Use "CASE" statements to map the identified component with its equivalent PSpice model.
8. Scan the "port - mapping" definition to identify the input and output net names and assign them to appropriate PSpice model terminals.
9. Loop until the end of architecture section is reached.

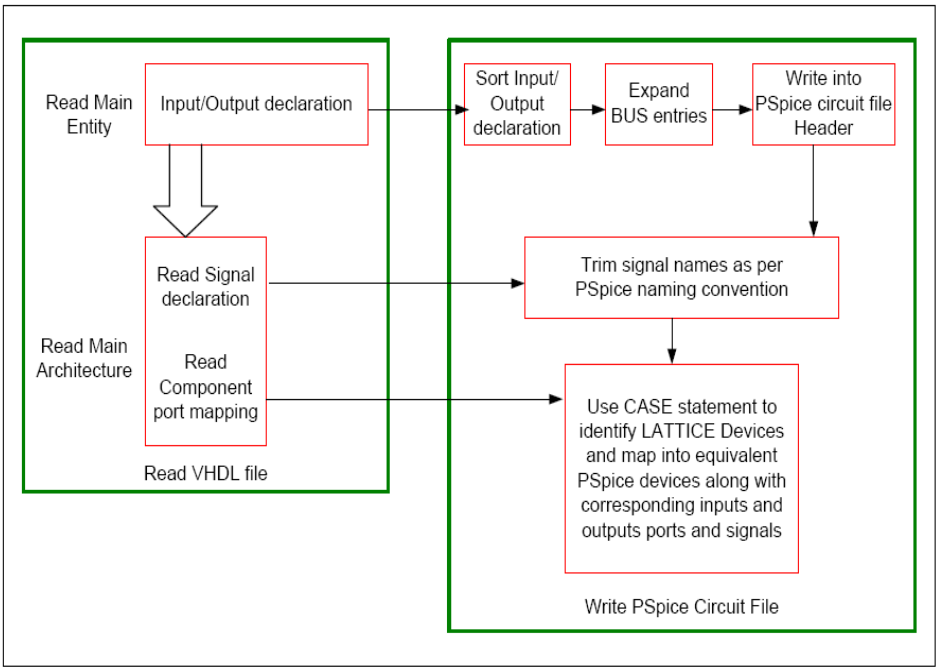


Fig. 2. Flow chart for VHDL-PSpice Conversion program

3. Mixed signal Design:

The ICM7555 and ICM7556 are CMOS RC timers providing significantly improved performance over the standard SE/NE 555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications.

Applications

1. Precision Timing
2. Pulse Generation
3. Sequential Timing
4. Time Delay Generation
5. Pulse Width Modulation
6. Pulse Position Modulation
7. Missing Pulse Detector

Two low cost CMOS ICs manage a 12 VDC ,current limited speed control circuit for DC brush motors .the circuit design uses PWM to chop the effective input voltage to the motor. use of cmos devices gives the benefits of low power ,minimal heat and improved longevity. the overall design is simple ,inexpensive and reliable ,and is useful in application such as embedded .

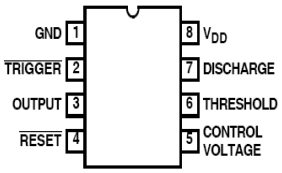


Fig1. ICM7555 (8 LD PDIP, SOIC)

Although the supply current consumed by the ICM7555 and ICM7556 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2

Circuit concept:

Low –cost DC Motor Speed control with CMOS ICs - A CMOS update of the popular -555 timer device is used because it draws much lower operating currents and then runs cooler and lasts longer in typing operating environments, by adjusting the wiper of the speed –control potentiometer, output-signal duty cycle ,or pulse width ,can be varied from 2% to 98%.operating frequency is fixed at 20khz,to remain in the inaudible range.

Two signals are generated: The PWM signal ,and a direction signal (high=forward ,low=reverse).these signals become inputs to the TC4469, a CMOS quad MOSFET driver .its logic inputs allow proper output chopping and commutation. Similar way using ICs&transistor PWM Driving DC Motor using embedded Technology and its implemented on VLSI Technology(Fig2 &3)

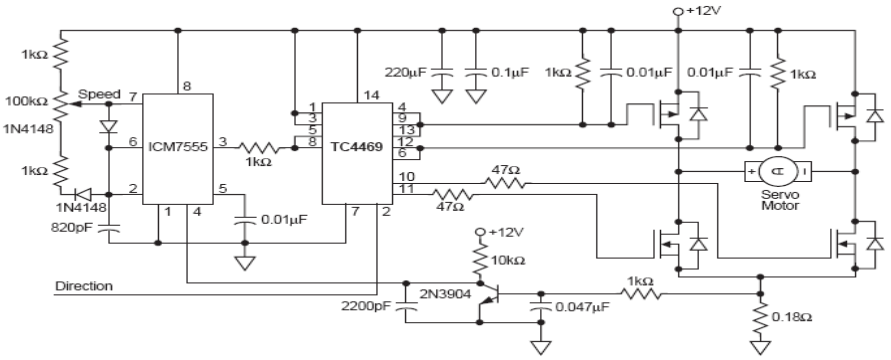


Fig .2. 12VDC Speed control and current limit

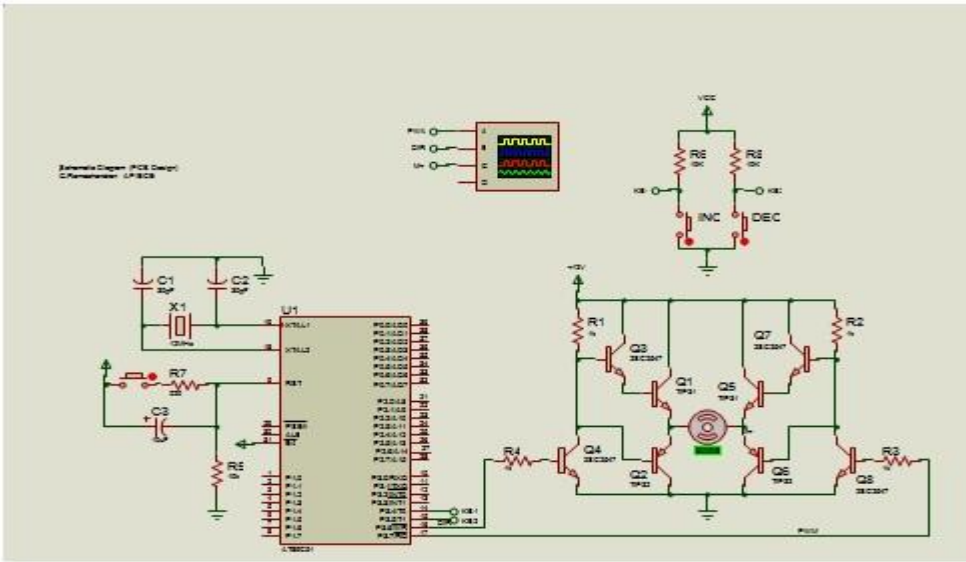


Fig 3. PWM Driving DC Motor

Observe the pulse train applied and motor voltage on the osciloscope.You can change the motor speed using the toggle buttons during simulation This design demonstrates the use of an AT89C51 to control a DC motor using PWM Four Transistors-2SC2547

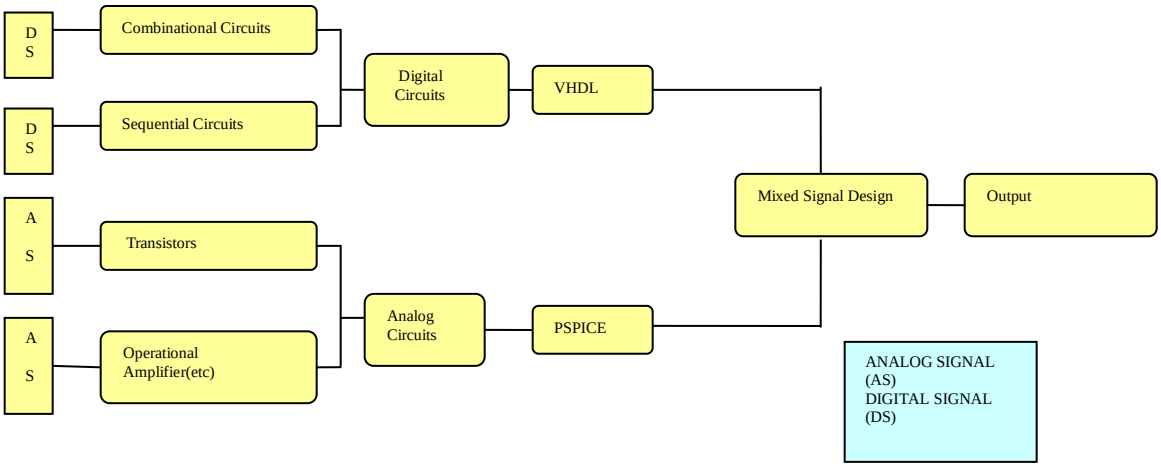


Fig 4 Mixed Level and Mixed Signal Simulation using PSpice and VHDL

3.1Schematic Diagram

3.1.1RTL Schematic

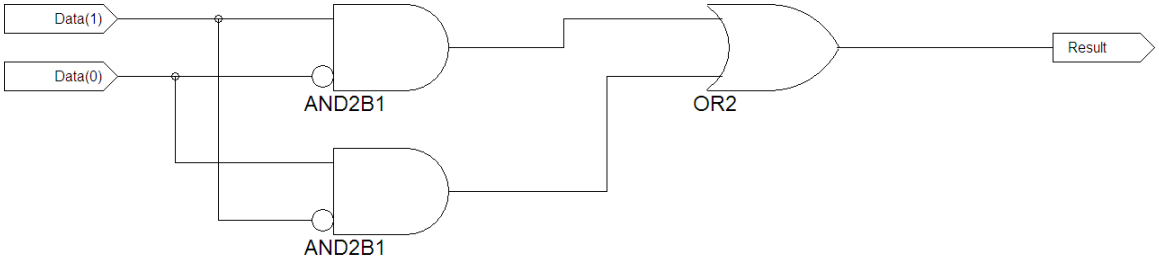


Fig 3.1.1. Basic RTL Schematic

3.1.2Technology Schematic

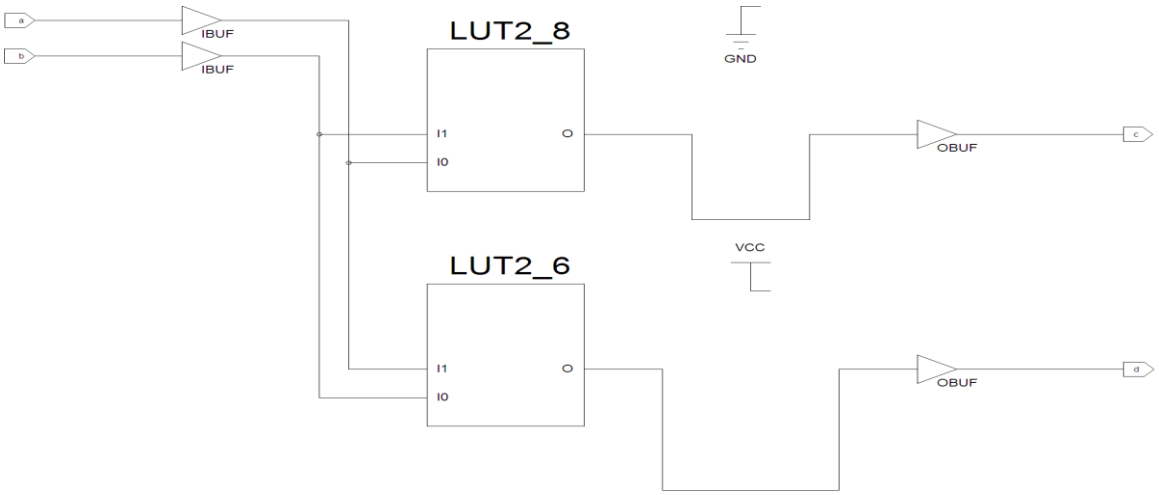


Fig 3.1.2LUT 2 INIT 6 &LUT 2 INIT 8 Technology Schematic

4. Simulation Results:- Mixed level &Mixed signal simulation using VHDL

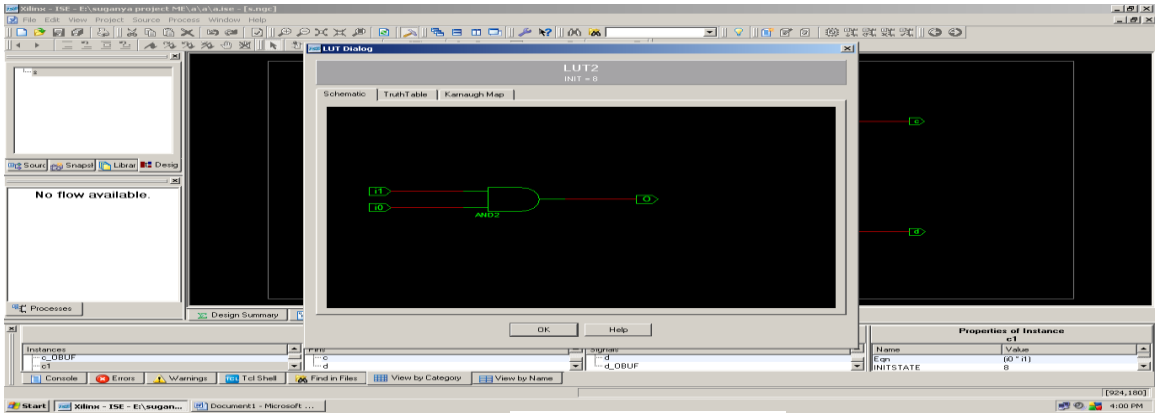


Fig 1. Basic AND, NOT and OR gates

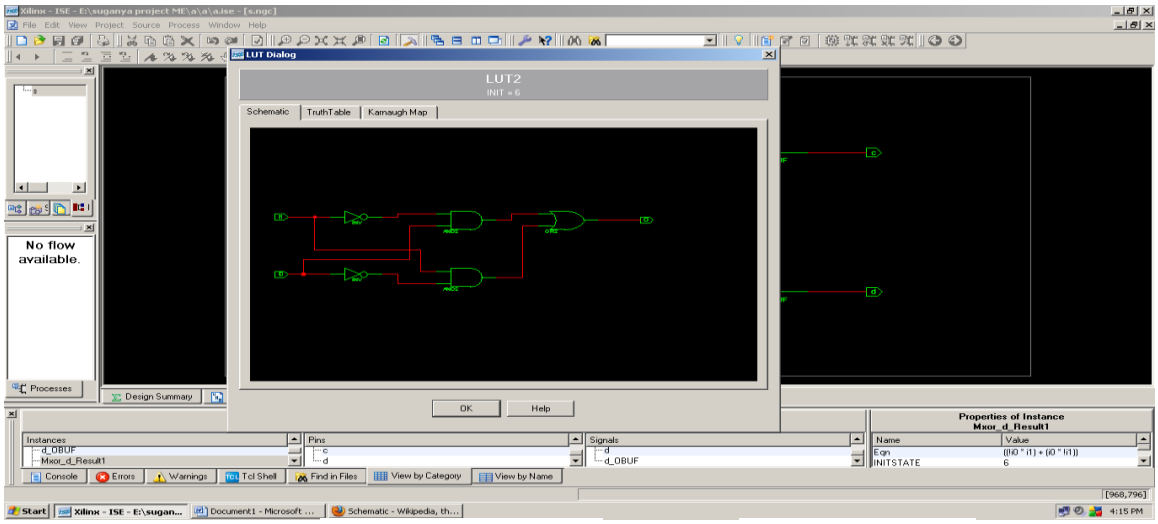


Fig 2. Basic AND, NOT and OR gates Universal ie NAND or NOR gates

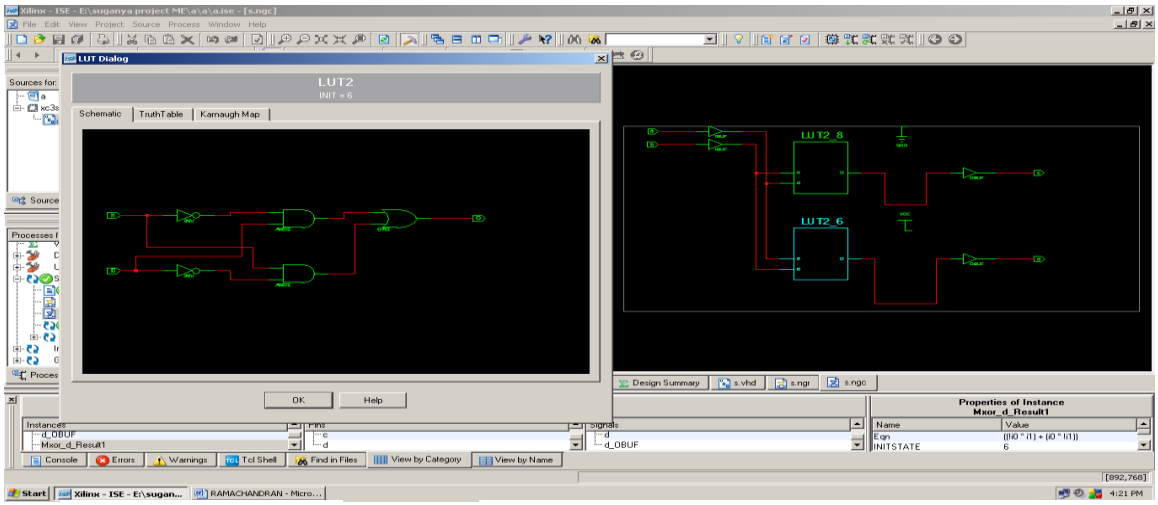


Fig 3. Basic AND, NOT and OR gates Universal ie NAND or NOR gates& Combinational: X-OR GATE or X-NOR Gate

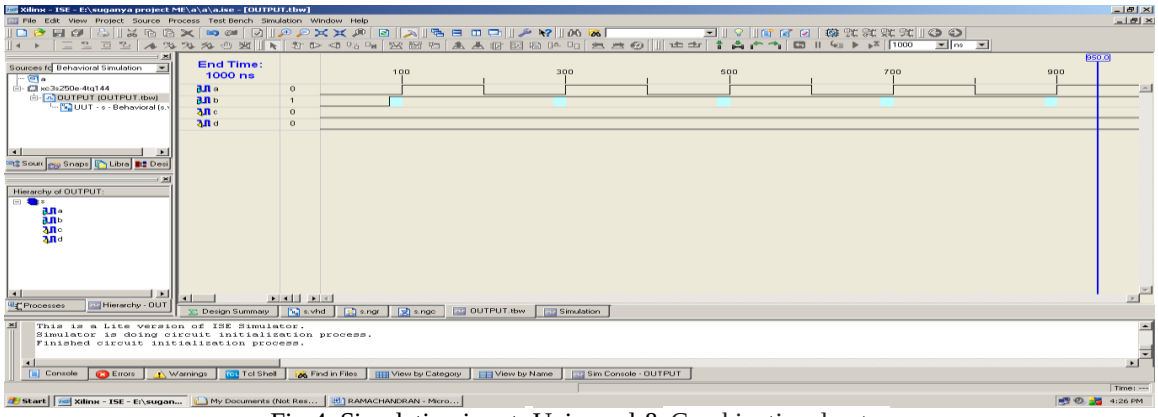


Fig 4. Simulation input: Universal & Combinational gates

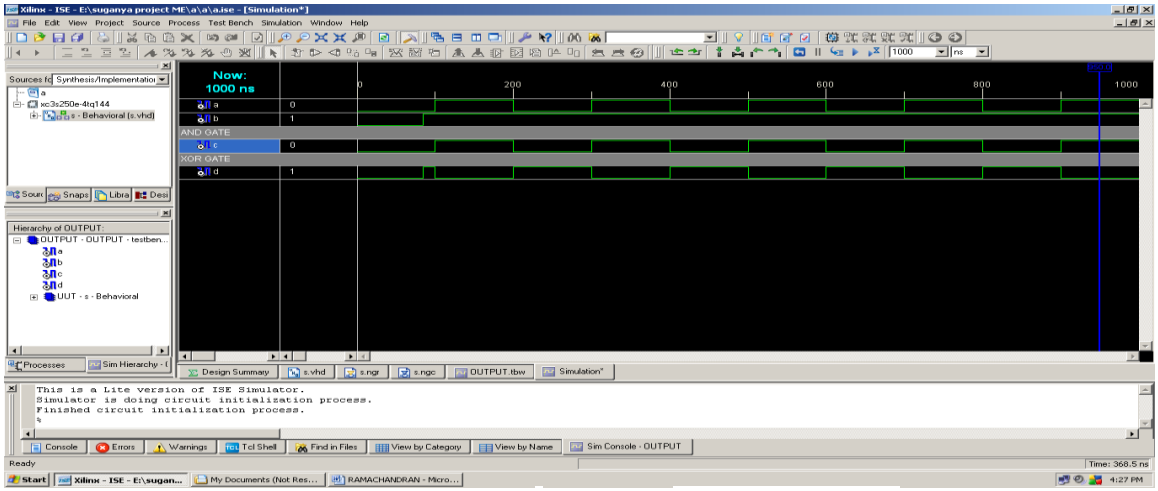


Fig 5. Simulation Output: Universal & Combinational gates

5.Dsh: Schematic: Mixed level &Mixed signal simulation using PSPICE

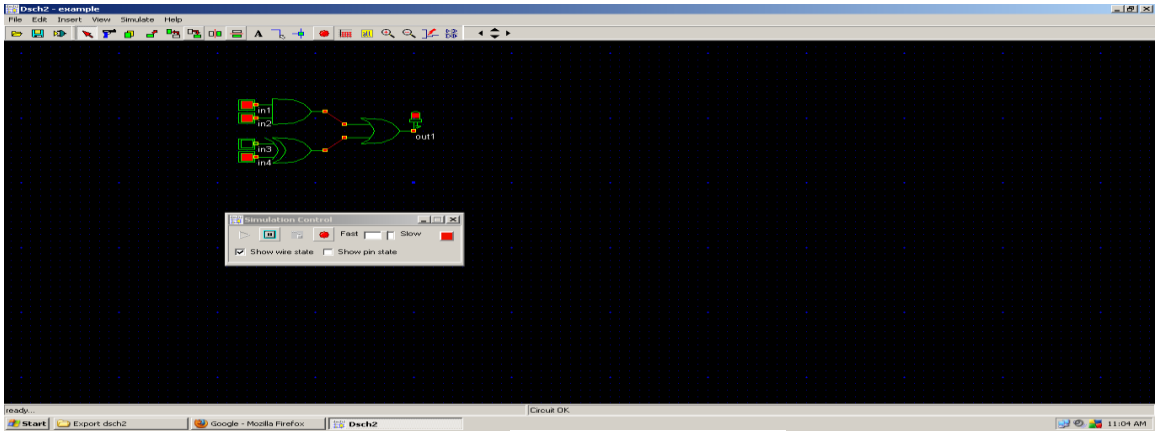


Fig 1. Basic AND, NOT and OR gates

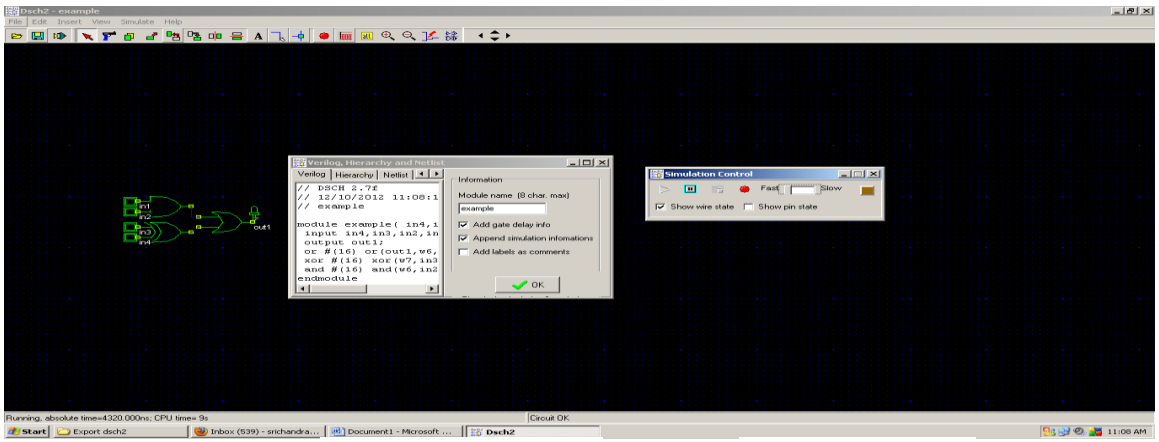


Fig 2. Basic AND, NOT and OR gates Universal ie NAND or NOR gates

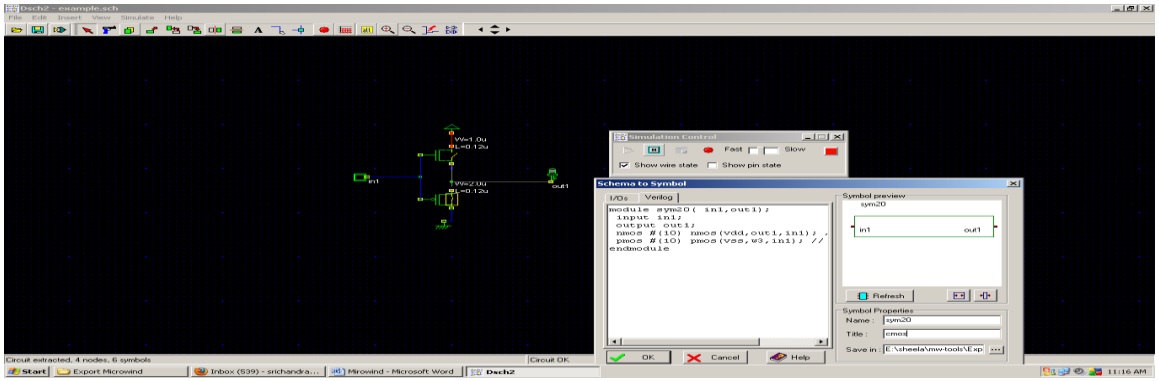
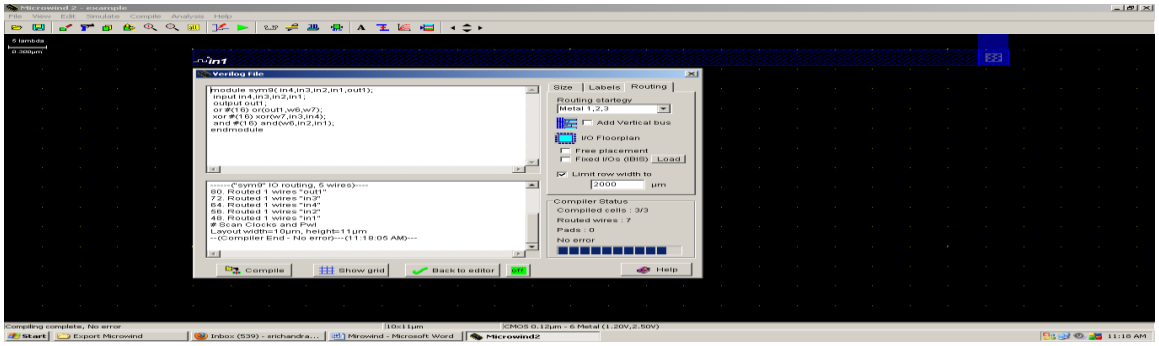


Fig 3. CMOS(Basic AND, NOT and OR gates Universal ie NAND or NOR gates& Combinational: X-OR GATE or X-NOR Gate)



Execution of **CMOS** (Basic AND, NOT and OR gates Universal ie NAND or NOR gates& Combinational: X-OR GATE or X-NOR Gate)

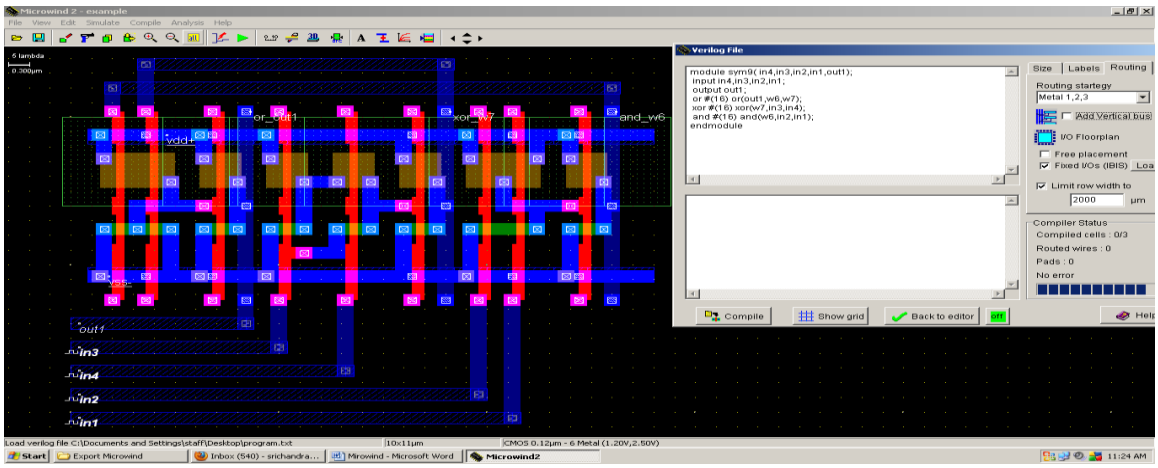


Fig. 3. Block diagram of the design from CMOS Layout

5. Conclusion

Prior to the proposed design methodology, circuit designers had to duplicate the output signals (Johnson counter) from the FPGA with clock generator functions in PSpice. Subjecting the entire design to various input conditions and performing total system verification at the design level was difficult. The new design methodology and the additional tools (*interfacing software and PSpice device library for Lattice devices*) enabled the simulation of the VHDL model in PSpice A/D. It was also possible to precisely model the arrival times of input signals from the VHDL model in PSpice, which in turn produced accurate conversion of DC power to AC. Simulating the entire design at the PCB level allowed engineers to study the behavior of the analog circuits when controlled by the FPGA. The simulation results presented in the previous sections asserts the following

Accurate conversion of the gate level VHDL description into an equivalent PSpice sub circuit file The customized PSpice library of digital devices for the LATTICE MACH 111 technology were modeled accurately

The overall time to run simulation is increased due to the gate level representation of digital logic and the clock interval of the master clock.

Total system verification at the design level was made possible by co-simulating digital circuits modeled in VHDL along with discrete analog components in PSpice. Violation of timing conditions, analog to digital interface problems etc. are some of the typical issues that can be addressed earlier in the design cycle due to
the proposed design methodology.

In this work the possibility of mixed level simulation in PSpice A/D using VHDL was investigated. A new design methodology to simulate synthesizable VHDL models in PSpice A/D was proposed. It combined traditional and top down design methodology in one simulation environment. To achieve this goal additional tools (interfacing software and PSpice device libraries) were required. These tools were developed and their functionality were verified in a practical application (case study). The new design methodology enables verification of mixed signal PCBs that contain PLDs like FPGAs, CPLDs, etc. at the design level and introduces an additional check-point before taking the design to hardware. Overall, it showed an effective way to verify the functionality of the mixed signal design. In examples such as the one studied in this work, different design teams work on different sections of the same design, namely analog and digital. In such situations, where the possibility of error introduced in the design process is high, this proposed methodology provides an easy and simple way to verify the functionality of the entire mixed signal design and provides an excellent chance to identify integration problems much earlier in the design cycle. However, the disadvantage is the increase in overall simulation run time.

6. FUTURE WORK

The following areas were identified for further research , Increased simulation time. Using gate level VHDL netlist can become a bottleneck if the number of gates in the netlist exceeds a few thousand. In order to reduce the simulation time, further investigation on behavioral simulation methods of the VHDL code in PSpice is necessary.

MATLAB Simulink® is a system level simulation tool. It has the ability to simulate electro-mechanical systems and it can integrate with PSpice simulation engine. If these abilities can be combined with the new design methodology then it can provide co simulation between system level, circuit level and HDL based designs.

Improved graphical user interface. The proposed methodology involves repeating a sequence of commands in each of the EDA tools, which can be scripted and automated. In doing so, a lot of details can be hidden from an end user and this would increase the appeal of the solution.

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