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BJT-Based Low Noise Amplifier Simulation Design for 900 MHz Frequency Range

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ABSTRACT
In this work, a simulation of a one-stage low-noise amplifier was designed to operate at a frequency of 900MHz using both lumped and strip-distributed circuits. The output results of the lumped circuit were compared with those of the distributed circuit. Differences in the reflection coefficients and gain were found while keeping the noise figure low. Also it is found that adding a series resistance to the transistor collector improved the stability of the transistor.

KEYWORDS:*BJT, low noise amplifier, simulation, refraction coefficients, noise figure.*

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I. INTRODUCTION

The signal receiver usually consists of two main parts, antenna and the Low Noise Amplifier (LNA). The LNA is used in radio frequency or microwave receiver applications because it has a very low Figure Noise NF. It amplifies the small signal that the regular amplifier cannot detect and amplify. The LNA consists of a transistor and matching circuits that are used to convert the impedance from a low value to a high value or vice versa, eliminate reflections, improve the circuit's performance in terms of gain or noise level, etc. The matching circuits are located between the antenna output and the transistor input, as well as between the transistor output and the circuit load, [1]. The transistor is the cornerstone in the design of low-noise amplifier circuits (LNA), and transistors of the BJT and FET types or similar types are usually used in their working mechanism to achieve the slightest noise and the best amplification. In addition to the input matching circuit and the output matching circuit, the transistor is, therefore, an important part of the design. It must have good specifications regarding high gain and low noise and consume little current. Also, when choosing the transistor, the matching must be possible at the frequency at which it operates, and this is done through the datasheet for the transistor, which is prepared by the manufacturer and provides all the essential information about it. There are some general requirements for choosing the ideal transistor in amplifiers, such as; low bias supply voltage (~2volt), low current consumption (<10 mA) approximately. High gain (≥15 dB) as much as possible. Low NF (≤2 dB), unconditional stability. Its dimensions should be as small and cost-effective as possible [2]. Additionally the frequency range in which it operates. BJT amplifiers typically have a low input voltage noise density, but a relatively high input current noise density, with a bandwidth of less than 30MHz. To decrease voltage noise, IC circuits are designed with a high collector current in the input state since the voltage noise is inversely proportional to the square root of the collector current. The current noise is proportional to the square root of the collector current, so low external power and source resistance are crucial for optimal noise performance. Voltage noise in BJT amplifiers is more pronounced when the source resistance is under 200Ω. Increasing the input bias current will also raise the current noise. Therefore, BJT amplifiers are better suited for low-input impedance applications [3]. Recent literature about LNA, such as Kunar et al., introduced a new BJT-based LNA design optimized for 5G frequencies, focusing on enhancing efficiency and reducing noise figures [4]. Zhang and Chen provide a study of advanced design techniques for improving noise performance in BJTs for high-speed communication systems [5]. M. Green et al. This work explores integration techniques for designing BJT LNAs that achieve low noise and power efficiency for portable devices[6].

This work aimed to design a single-stage low-noise amplifier circuit that operates at 900MHz. Then, using specialized equations, the components of the lumped circuit were converted into a strip-distributed circuit. The output results of the designed lumped circuit were compared with the output results of the distributed circuit at the operating frequency to assess its stability.

II. Method and Materials

The design began with using the Office Microwave-2000 program (MWO) to design and analyze microwave circuits and preparing a Matlab program to calculate the mathematical equations related to the dimensions of the chip. After that, the lumped circuit was created from the original elements, and necessary measurements were taken. Next, a distributed circuit was prepared from the assembled circuit in the form of a microstrip. The work was divided into three parts: The first part involved designing the initial model of the lumped circuit for a low-noise amplifier operating in microwave frequencies and its matching circuits with the help of the MWO program. The second part involved converting circuit components into strip elements distributed on an Epoxy substrate.

LNA Circuit Simulation:

At this stage, an LNA was designed using BJT type (HO405-2A) & (T605108A) at 900MHz frequency, a lumped circuit was formed using a BJT transistor, and the matching stage was carried out to obtain the lowest reflectivity using the (MWO) program and the Smith chart to convert the components of the collector circuit into a distributed circuit. The lumped circuit was transformed into a distributed circuit by calculating the dimensions of each component, such as inductance (L), resistance (R), and capacitance (C). A Matlab program was developed using the conversion equations from [7], and [8]. The required input data included the substrate thickness h=1.5 mm, the chosen dielectric Epoxy with εr =4.37, the input impedance Zm=50 ohms, the thickness of the copper conductor t ≤0.5 µm, and the specific resistance $\rho=1.7\times10\text{-}6\ \Omega.cm$.

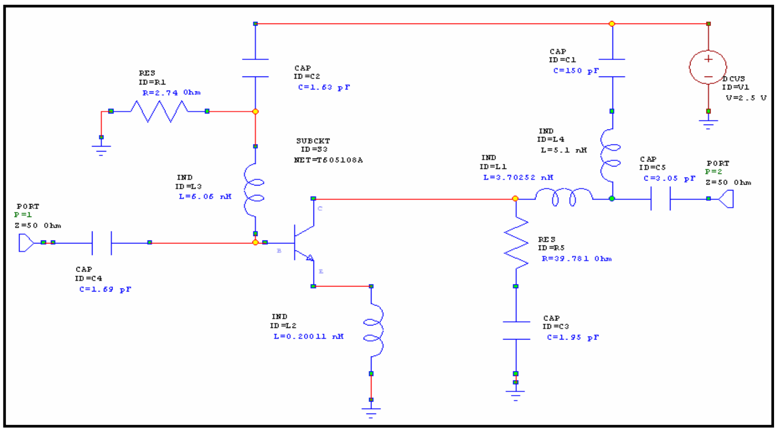

Figure 1: **The lumped LNA circuit with BJT**

The width of the circuit elements were listed in Table 1, and the lengths of the elements were determined for each values of inductance, resistance, and capacitance [9].

Table 1: The width of each elements of the distribution circuit

Epoxy	tan δ	Z_m (ohm)	W_R (mm)	W_L (mm)	Wc (mm)
ε_r=4.37	0.0366	50	2.88	1.17	15.65

The output results of the distributed circuit after converting are shown in Figure (2).

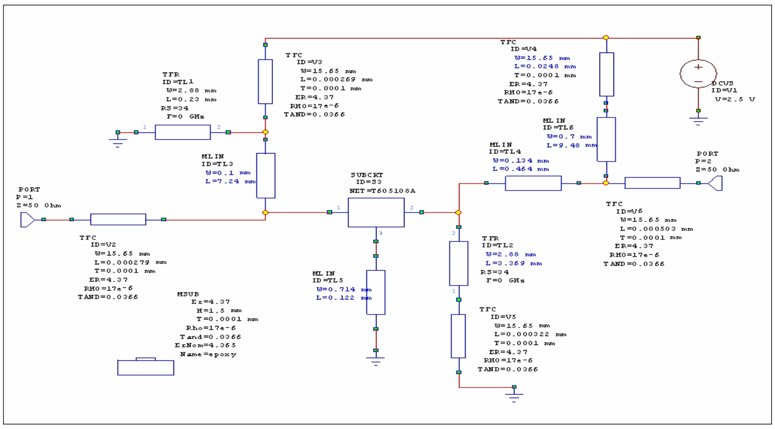

Figure 2:The distributed LNA circuit with BJT

III. Results and Discussion

Figure (3) shows Smith chart of the lumped and the distributed circuit. The value obtained for the matching when simulating the circuits for both the input and output impedance close to (50Ω). The circuit's performance is good at the operating frequency. This means that the input circuit is compatible with the transistor input on the one hand, and the transistor output is compatible with the circuit output on the other hand.

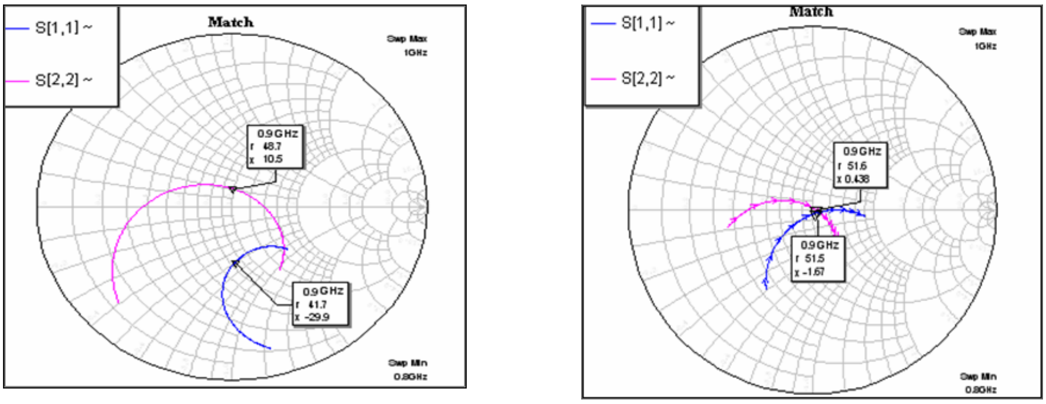

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Figure 3: Smith's chart of a LNA circuit (a) lumped circuit (b) distributed circuit

Figure (4) displays the S11 reflection coefficient at the input, and Figure 4-a shows the lumped circuit's lowest value at the center frequency of 900MHz, which is -9.8dB. At 1GHz, it increases slightly to -8.3 dB. This indicates that the matching circuit performs best near 900MHz. The S22 reflection coefficient similarly affects the matching circuit's performance at the output, showing the efficiency between the transistor output and the circuit's output end. A lower S22 value is better, and from Figure 2.4, the lowest S22 value is -19.4dB at the center frequency of 900MHz. The S21 coefficient represents the forward gain factor S21 for the lumped circuit, whose value ranges from 13.4dB to 13.9dB at the central frequency of 900MHz; it had an acceptable value for one stage 14.6dB.

For the distributed circuit Figure 4-b, the S11 indicates good matching at the center frequency of 900MHz with a value of -32.6dB, whereas the lowest S22 value was -35.6dB at a frequency of 900MHz. Additionally, the forward gain coefficient S21 ranges from 12.4dB at 850MHz to 12.5dB at 950MHz, with the highest value at the center frequency of 900MHz, which is 12.9dB an acceptable performance for a single-stage amplifier circuit.

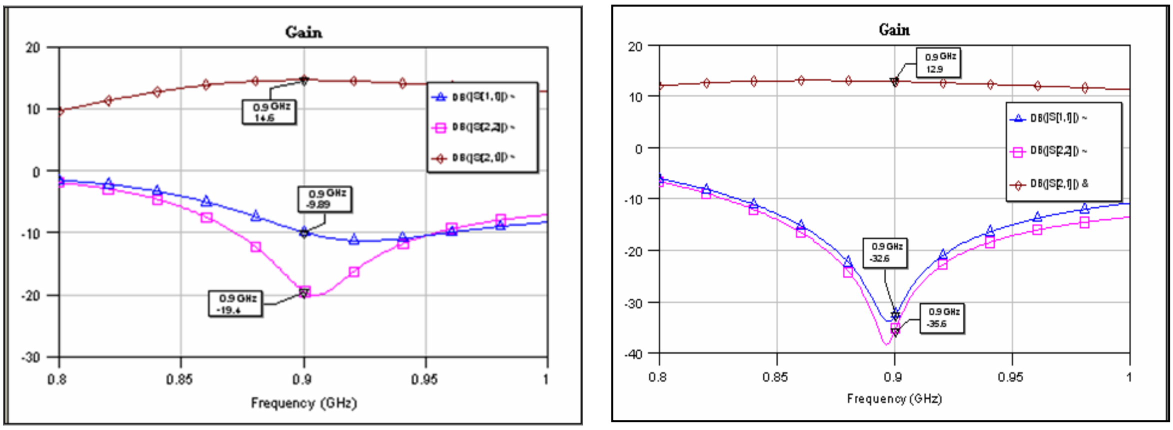

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Figure 4: The S-parameters S11, S22, S21 for the LNA (a) lumped (b) distributed circuit

Figure (7-a) for the lumped circuit shows the change in the noise level with frequency. Its value ranged from 6.6dB at 800MHz and gradually decreased with increasing frequency to 3.8dB at 1GHz, while it was 5.0dB at 900MHz. This value is expected from a BJT transistor, as a high noise figure characterizes this type of transistor. Figure (7-b) for distributed circuit shows the change in the noise figure with frequency, as its value ranged from 4.5dB at 800MHz and decreased to became 2.9dB at 1GHz, while it was 3.4dB at 900MHz. This value is less than in the lumped circuit.

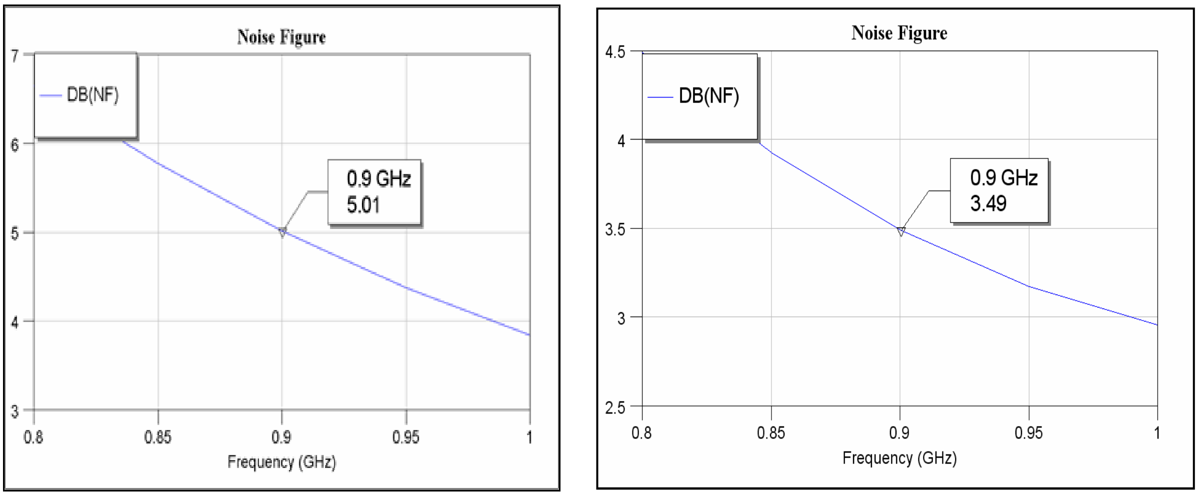

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Figure 7: Noise figure of the LNA circuit at 900MHz

The stability factor K is essential to the amplifier's stability. The greater its value is than one, the more it is considered evidence of the amplifier's unconditional stability. Accordingly, particular importance has been given to stability in the circuit design at this frequency of 900MHz.

Figure (8-a) shows that the K value 1.06 at 900MHz for lumped circuit, and 2.68 at the operating frequency 900MHz for distributed circuit, as shown in Figure (8-b).

The simulation results for design of one stage LNA can be summarized in the following Table (2).

Table 2: The main results for the LNA with BJT

LNA	Work type	Transistor	Frequency (MHz)	Gain (dB)	Noise Figure (dB)	Stability (K)
One-stage	**Simulation**	**BJT**	**900**	**12.5**	**3.4**	**2.6**

IV. CONCLUSION

The previous results indicate that there are some differences in the output values between the distributed circuit and the lumped circuit, such as the S11 and S22 coefficients, as well as the gain of S21. These differences are due to integration in the operating frequency and the change in the operating point of the transistor. In the design of a single-stage LNA, it's crucial to keep the noise figure (NF) as low as possible. In this design, it was observed that connecting a series resistance with the transistor collector helps improve stability, but it may reduce the gain. As a result, it's not preferable to use resistors in the input matching circuit because they increase noise. Instead, it's better to use series inductance and shunt capacitance.

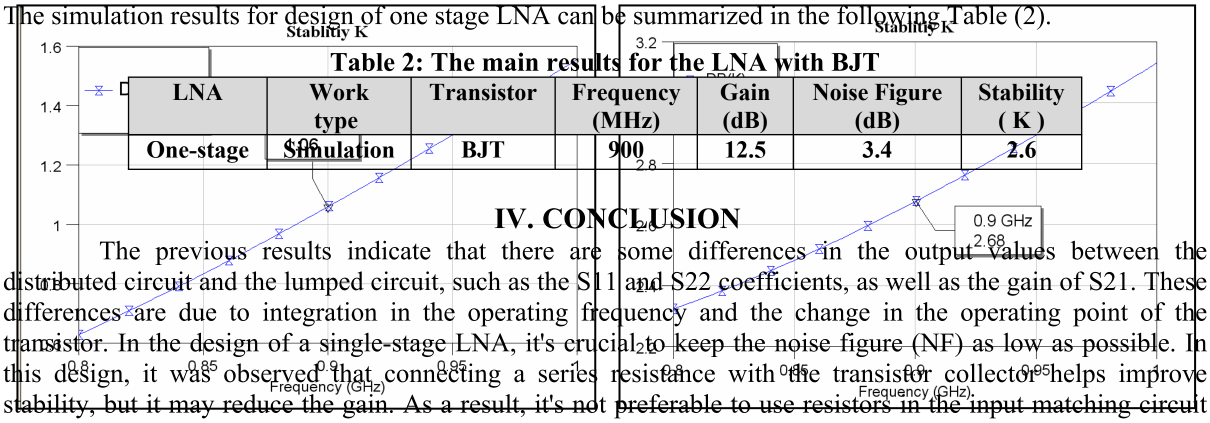

Figure 6: The stability curve (K) of the LNA circuit

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