Embedded Web Server using Soft Processor on FPGA Platform

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Abstract
This paper describes the design of Embedded Web Server on Soft core, a configurable RISC processor available on Spartan 3a FPGA kit. An Embedded Web Server is used to monitor and control embedded application using any web browser. Embedded web server does not need high configuration computers, hence replaces the conventional heavy weight traditional web servers providing high speed low power consumption, reduced cost, complexity, footprint and size. Web server application is designed using Xilinx Platform studio. The embedded web server can communicate with web browser using TCP/HTTP and supports I/O communication. The Web server application runs on XMK Xilinx Microkernel operating system.

Keywords— Micro Blaze, FPGA, IP, TCP/HTTP, EDK, SDK

I. INTRODUCTION
Embedded System encounters numerous developments that makes people work completely on Web based configurations and services. The web server is the central functional unit to get access on an embedded system via web browser. Basically a web server accepts requests from client and serves responses through HTML pages with linked objects.

Popular web servers are Apache web server, IIS, Sun Java web server etc. These heavy weight servers are costly and support only certain platform. To overcome these drawbacks, embedded web server that features high speed, reduced cost, complexity and size can be built.

II. TECHNICAL OVERVIEW
A Field Programmable Gate Array (FPGA) is a device having programmable logic cells known as Configurable Logic Blocks (CLB). Programmable interconnections are used to connect them. A CLB has a Look-Up Table (LUT) that can be configured to give a specific type of logic function.

A. IP Cores
The design of complex systems in FPGA is simplified by libraries of predefined complex functions and circuits that have been tested and optimised to ease the design process. These predefined circuits are commonly known as Intellectual Property cores or IP cores. The two types of IP cores in FPGA are Soft cores and Hard cores.

Soft cores are implemented using general purpose FPGA logic cells. They are in the form of HDL and needs a license, GPL or Proprietary. MicroBlaze, Nios, PicoBlaze are examples of Soft core. Hard core are synthesized dedicated parts of IC that can be initiated in design. PowerPC of Xilinx is a Hard core processor.

A. Soft Core Processors
Xilinx offers PicoBlaze and MicroBlaze soft core processors with Xilinx ISE. Altera provides Nios core with Nios IDE.

1)PicoBlaze: PicoBlaze is a 8-bit soft processor core provided as a free, source-level VHDL file with royalty-free re-use within Xilinx FPGAs.

2)Nios: Nios is a soft processor defined in a hardware description language that can be implemented in Altera's FPGA devices by using the Quartus II CAD system.

3)MicroBlaze: MicroBlaze is a 32-bit RISC Harvard architecture soft processor core with a rich instruction set optimized for embedded applications.

Category	PicoBlaze	MicroBlaze	Nios II (Fast Core)
Maximum MHz	200 (FPGA)	200 (FPGA)	200 (FPGA)
ASIC/FPGA Technology	Spartan 3	Spartan 3a DSP	Stratix and StratixII
Reported DMIPS	100 DMIPs	166 DMIPs	150 DMIPs
ISA	8-bit RISC	32-bit RISC	32-bit RISC
Cache Memory (I/D)	Upto 8 KB	Upto 64 KB	Upto 64 KB
Floating Point Unit (optional)	-	IEEE-754	IEEE-754

Table 1 Comparison Of Soft Core Processors

III. HARDWARE PLATFORM

The Spartan-3A DSP 3400A Development Platform is built with Spartan-3A DSP XC3SD3400A device that provides significant resources such as 126 embedded DSP blocks for implementing high performance video processing systems and co-processors. Figure 1 shows Spartan 3a DSP development kit [12].

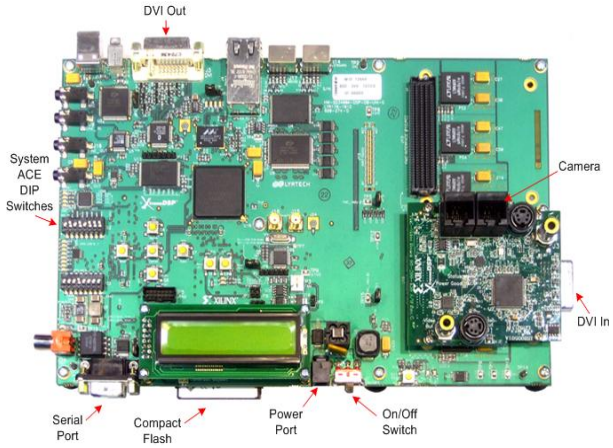

Fig. 1 Spartan-3A DSP 3400A Development Platform

Figure 2 shows MicroBlaze block diagram [10]. The components of primary interest are Spartan 3a DSP FPGA, DDR2 SDRAM, DB9 RS232 connector, Compact Flash, RJ45 Ethernet PHY. The base platform includes following Processor IP blocks:

- MicroBlaze 32-bit Soft Microprocessor
- Local Memory Bus (LMB)
- LMB Block RAM Controller
- Block RAM Block Memory
- Processor Local Bus (PLB)
- XPS Uartlite

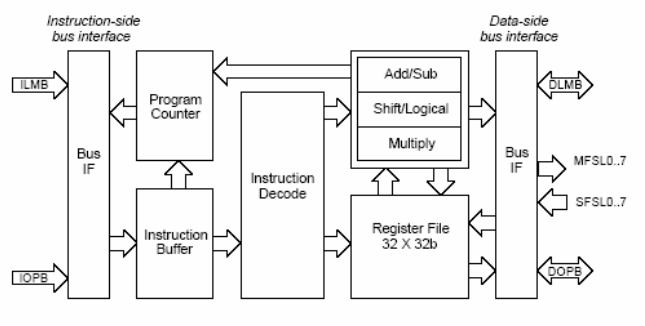

Fig. 2 MicroBlaze Block Diagram

MicroBlaze has separate bus interface units for data and instruction access. Each bus interface unit is further split into Local Memory Bus (LMB) and IBM's On-chip Peripheral Bus (OPB). The LMB provides single-cycle access to onchip dual-port block RAM. The OPB interface provides a connection to both on and off- chip peripherals and memory.

A. 10/100 Ethernet

The onboard Ethernet PHY KS8041NL needs a single 3.3V supply. 10base-T/100base-TX physical layer transceiver provides an interface to transmit and receive data. Ethernet clock 25MHz is given from FPGA.

IV. SOFTWARE DESIGN

The Web server program running on MicroBlaze soft processor can be designed using the Embedded Development Kit (EDK). Xilinx Platform Studio (XPS) of EDK software tool is used to create project file and control the hardware and software development of the MicroBlaze system.

A. Steps to create XPS project

The steps to create embedded system hardware platform using XPS of EDK software tool are as follows:

- Create a new project file using BSB (Base System Builder) wizard
- Microprocessor Hardware Specification File (MHS), a textual schematic of the embedded system is created
- Microprocessor Software Specification File (MSS) that specifies the driver software of all the components of MicroBlaze is created.

B. Steps to create SDK application project

The steps to create application project using SDK are given below.

- Export the hardware design created in EDK to SDK
- Create application project and include library of routines in your application
- Download the hardware bit stream to FPGA device
- Download the application and run the software executable

V. CLIENT-SERVER COMMUNICATION

A web server is special kind of a file server. A web browser requests a file from a web server by issuing the HTTP GET request. The web server receives the HTTP GET request and accesses its file system for the requested file. The web server generates the HTTP response which is comprised of an http header and the requested file and transmits it to the browser. If the requested file is not accessible a special error response is generated and transmitted to the browser

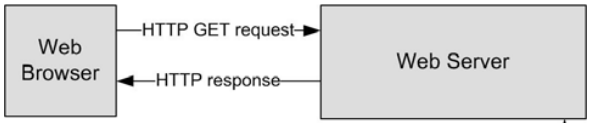

Fig. 2 Client-Server Communication

VI. FUNCTIONALITY

The web server designed displays a web page with following operations:

- Static HTML page hosting
- LED displays Hex to Binary value
- HTTP File transfer
- Push buttons value displayed in binary

VII. CONCLUSION

The system designed allows us to control and monitor the embedded system anywhere away from the field of work. It uses light weight TCP/IP protocol to communicate. The data rate achieved by the embedded web server for communication is very low that results in slow loading of webpage. If caching of DDR for the web server application is used, the response of time to incoming requests is still very short.

Embedded web server can further implement multitasking of tasks using FSL (Fast Simplex Links) bus interface. A Fast Simplex Link (FSL) interface provides a fast connection from the OPB MicroBlaze Debug Module (MDM) to the MicroBlaze processor.

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