

Dielectric Dependent Absorption Characteristics In Cnfet Infrared Phototransistor

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ABSTRACT In future infrared photodetectors, single-walled carbon nanotubes (SWCNTs) are considered as potential candidates due to their band gap, high absorption coefficient ($10^4 - 10^5 \text{ cm}^{-1}$), high charge carrier mobility and ease of processability. The SWCNT based Field Effect Transistors (CNFETs) are being seriously reviewed for applications in optoelectronics. In the proposed work optically controlled back gated CNFET is modeled in Sentaurus TCAD. Transfer characteristics of the device are analyzed under dark and illuminated conditions at varying chirality for SWCNTs. Small deviation in SWCNT chirality shows significant change in channel current. Work is further continued with an analysis for high- κ (25) Hafnium Dioxide (HfO_2) thin film ($\sim 10 \text{ nm}$) as gate dielectric. CNFET integrated with HfO_2 dielectrics exhibits superior performance with a significant rise in channel current. Precise two dimensional TCAD simulation results and visual figures affirm that the ON state performance of CNFET has significant dependency on the dielectric strength as well as width of the gate oxide and its application in enhancing the performance of carbon nanotube based infrared photo detectors.

KEYWORDS: Infrared Photo Detector, CNFETs, Hafnium compounds, High-k gate dielectrics, Semiconductor device modeling, TCAD Simulation.

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I. INTRODUCTION

Infrared photo detectors can be used for a variety of applications in the military, security, medical, industrial and telecommunication areas. Photo devices flexibility and broadening the photosensitive spectral range with low cost are foreseen to be the fundamental areas in promoting the relevancy of IR photodetectors [1]. Amongst the various preferred detector materials for infrared light, SWCNTs are being seriously considered as one of the potential candidates due to its outstanding electrical, optical, thermal and mechanical properties. Researchers have demonstrated that SWCNTs show strong absorption in the IR ($\approx 10^5 \text{ cm}^{-1}$), [2, and 3] due to high charge carrier mobility, 1D structure and high aspect ratio of SWCNT. In particular, SWCNT based planar photoconductors devices are of deep research in recent years due to their customizable electronics properties and 2D architecture. Also the same existing CMOS structure can be reused in SWCNT based phototransistors due to their compatibility with conventional MOSFETs, potentially enabling their on-chip integration, and multifunctional optoelectronics. SWCNT's can be integrated as channel in conventional MOSFETs to get scaled MOSFETs known as CNFET. SWCNT acts as the channel in CNFET and is responsible for transport mechanism. Still the performance of infra-red SWCNT phototransistors has thus far been inferior compared to other IR photodetectors comprised of different nano structured materials regardless of their potential[2, 4]. One of the main reasons for CNFET's low performance can be attributed to relatively low dielectric and larger thickness of SiO_2 gate oxide. Steep switching between ON and OFF states for CNFET can be attained by the incorporation of thin high dielectrics gate oxide. High dielectric gate oxides and SWCNT channel interface develops with reduced dangling bonds and hence does not degrade the carrier mobility in SWCNT channel. [5]

In this proposed work, possible impact of high- κ gate dielectric HfO_2 on CNFET phototransistor is studied through TCAD simulation. The distinctive features of the CNFET device with high dielectric HfO_2 gate oxide are observed and measured with those of a CNFET with low dielectric SiO_2 gate oxide in terms of output characteristics and responsivity. In this simulation approach; 2D CNFET model is implemented including the principles of calculation of SWCNT charge, which is responsible for the current transportation. This charge developed on the SWCNT surface is due to the potential across SWCNT which is responsible for channel band

alterations [6]. The CNFET model considers SWCNTs with different diameter and channel length. This model is valid as long as the active channel SWCNT in CNFET phototransistor is behaving as semiconducting.

II. SWCNT THEORY

A. Optical Properties of SWCNT

SWCNTs are tiny, hollow cylinders constructed by rolling up a 2D graphene sheet. C_h around roll-up vector in graphene sheet and describes how the sheet is rolled up to form SWCNTs with varying diameter and different electronics properties.

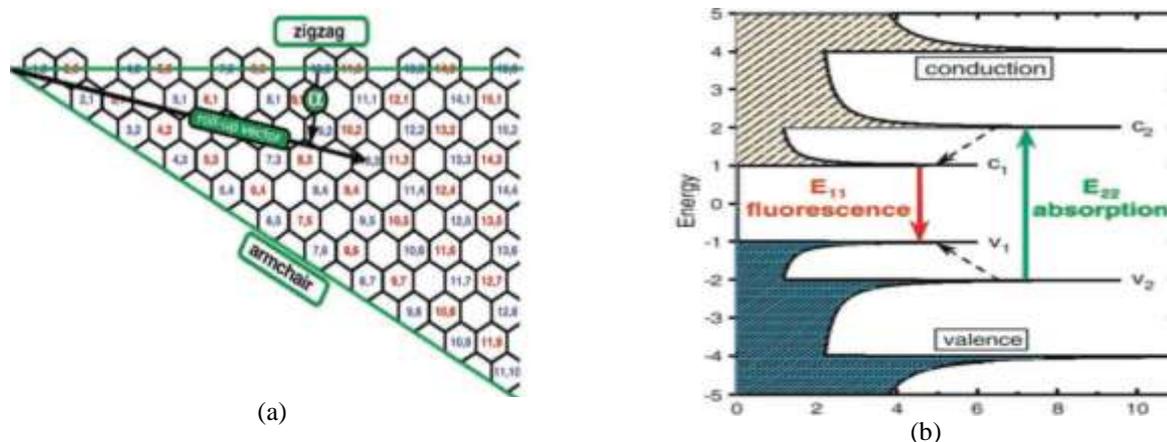


Figure.1 Carbon nanotube geometric structure (a) 2D Graphene sheet (b) Schematic density states in single walled carbon nanotube. [2]

Depending on the chirality of graphene cylinder, SWCNT diameter can be varied and SWCNTs results into semiconducting and metallic tubes shown in figure 1(a). Chirality vector, C_h with (n, m) defines diameter, bandgap and threshold voltage of SWCNT. Figure 1(b) indicates the presence of more than a few sub-bands with all energy bands having their maxima or minima at the same K points, indicates that nanotubes are unique material with direct bandgap. Such direct bandgap semiconducting SWCNTs due to their strong light absorption and fast light response over a broad band can be used in wide optoelectronics applications.

However with reduced dimensionality in SWCNTs many body effects dominate the light absorption. The most significant body effects amongst various optical properties are excitons, which are electron-hole pairs easily formed with much larger Columbic interaction energies. As seen in figure 1(b), photo excited electrons in SWCNT can be directly excited from valence bands to conduction bands for energies larger than its bandgap. But in the presence of excitons in semiconducting SWCNTs the optical absorption spectrum is completely altered; each band to band transition gives a series of sharp excitonic peaks. Free electrons and holes may be produced in lower subbands via excitations of excitons to higher energy subbands, followed by decaying to lower energy subbands to become free electrons and holes. In the first sub band, excitons has large exciton binding energy, hence it is usually difficult for them to decay to become free carriers. As inphotodetectors, external electric field or band bending due to doping are usually utilized to separate the photo carriers. In excitonic picture, larger electric field needs to be applied to disassociate the excitons into a free electron and hole [2].

B. Phototransistor Structure

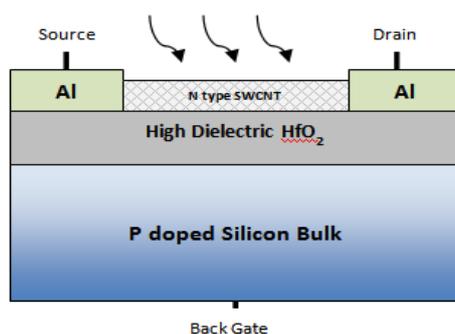


Figure. 2 Back Gated CNFET structure with High Dielectric HfO_2 gate insulation.

Schematic for the proposed back gated CNFET structure is shown in figure 2. The CNFET structure is of the standard back gated MOSFET with n doped SWCNT as active channel. Chiral numbers (n, m) which describe the different SWCNTs is responsible for its electronic properties.

$$C_h = na_1 + ma_2 \quad (1)$$

a_1 and a_2 are the unit vectors along the unit cell in 2D graphene sheet. Chiral vector C_h is the linear combination of lattice vectors a_1 and a_2 with m and n as integer indices [8].

In SWCNT, its diameter and bandgap are dependent on chiral indices and hence calculated with the help of (n, m) [9]. SWCNT diameter is derived by

$$d = \frac{\sqrt{3}a}{\pi} \sqrt{n^2 + m^2 + 2nm} \quad (2)$$

a is the distance between neighboring carbon atoms and its value is 0.142 nm [9]. Bandgap in SWCNT is dependent on its diameter [10] and is calculated as:

$$E_g = \frac{2aV_{pp\pi}}{\sqrt{3}d} \quad (3)$$

$V_{pp\pi}$ is the carbon π - π bond energy with value 3.033 eV [11].

The transport mechanism in SWCNT which is dependent on the intrinsic charge carrier concentration can be calculated as [11]:

$$n_{CNT} = \int_{E_c}^{\infty} D(E)f(E)dE \quad (4)$$

$D(E)$, $f(E)$ represents the density of states, Fermi-Dirac distribution in SWCNT respectively. $D(E)$ and $f(E)$ values are calculated using equations (5) and (6):

$$D(E)dE = 2 \sum_1^{All\ Bands} \frac{4}{\pi V_{pp\pi} a \sqrt{3}} \frac{E}{\sqrt{E^2 - E_c}} dE \quad (5)$$

E_c is the conduction band energy. The density of states value is calculated for the first sub band only since in SWCNTs the contributions of next level sub bands is negligible.

$$f(E) = \frac{1}{1 - \exp\left(\frac{E - E_f}{KT}\right)} \quad (6)$$

T is the operating temperature, K is the Boltzmann constant, and E_f is the first sub band Fermi level value in SWCNT. Substituting (5) and (6) in (4) to get the simplified expression for n_{CNT} :

$$n_{CNT} = N_C I \exp\left(\frac{-E_c}{KT}\right) \quad (7)$$

Where

$$N_C = \frac{8KT}{\pi V_{pp\pi} a \sqrt{3}} \quad (8)$$

And

$$I = \frac{1}{\sqrt{KT}} \int_0^{\frac{6E_c}{T}} \frac{(KT_x + E_c)}{\sqrt{x(KT_x + 2E_c)}} \exp(-x) dx \quad (9)$$

Channel current calculation is done using an expression in equation 9 [12].

In intrinsic SWCNT Fermi levels are zero on the source and drain side. By introducing n type doping in SWCNT, the nature of CNFET is affected and hence current along the channel also changes accordingly. Shift in Fermi level, E_f due to doping is given as [11]:

$$\Delta E_f = KT \ln\left(1 + \frac{N}{n_{CNT,i}}\right) \quad (10)$$

N represents the amount of doping concentration.

V_s , V_D be the source, drain bias respectively then the channel current I_{DS} is calculated using the Launder Equation as [15]:

$$I_{DS} = \frac{qkT}{\pi h} \left\{ \ln \left[1 + e^{\frac{\Delta E_f + q(\Psi_{CNT}(0) - V_s - \phi_0) - E_c}{KT}} \right] - \ln \left[1 + e^{\frac{\Delta E_f + q(\Psi_{CNT}(L) - V_D - \phi_0) - E_c}{KT}} \right] \right\} \quad (11)$$

h is Planck's constant and q is the electronic charge. $\Psi_{CNT}(0)$ and ϕ_0 is the surface potential on top and bottom of SWCNT.

III. SENTAURUS TCAD MODELING AND SIMULATION

Technology computer-aided design (TCAD) is a well-established discipline and optimization technique used in electronic device simulation in the market [14].

A. CNFET Model

All the required set dimensions of the device are listed in the table I.

TABLE 1 CNFET dimensions set for simulation

Dimension	Values (nm)
Channel Thickness (SWCNT diameter), t_{act}	Varying based on SWCNT diameter
Oxide thickness, t_{ox}	10 nm
Back gate thickness, t_{bulk}	100 nm
Source & Drain thickness , $t_{s,D}$	5 nm
Gate Length L_g (SWCNT length)	Varying
Source & Drain length , L_s & L_D	25 nm each
$Y_1=t_{bulk}$, $Y_2=Y_1+t_{ox}$, $Y_3=Y_2+t_{act}$, $Y_4=Y_3+t_{s,D}$	
$X_1=L_s$, $X_2=X_1+L_g$, $X_3=X_2+L_D$	

Following it, to develop the simulation model, an ordered description of the statements loaded in sde_dve.cmf file and region wise doping styles and doping concentration are defined and listed in table II.

TABLE II Region wise doping concentration

Region	Dopant	Doping Concentration
S _i Bulk Gate	Boron (B)	1×10^{16}
SWCNT channel	Phosphorus (P)	1×10^{17}

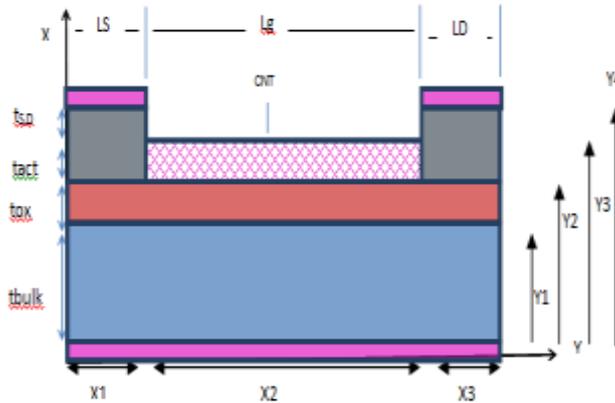


Figure.3 Schematic of 2D CNFET structure for simulation

Figure 3 depicts the schematic of the corresponding 2D CNFET structure established during simulation.

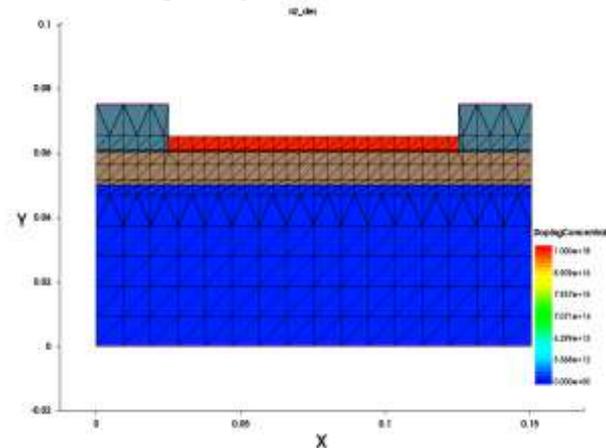


Figure4 Varying mesh across CNFET regions

The electrical properties of CNFET are based on the simultaneous solution of various partial differential equations. During the device simulation calculation of these equations is done at the locations of intersection points in the mesh defined across various regions of CNFET shown in figure 4.

As seen in figure 4, active layer is defined with more dense mesh in order to obtain optimized simulation results considering speed and accuracy of TCAD software. The complete 2D CNFET structure established in SDE tool is shown in figure 5, without any physical model applied to it. Therefore to carry out the CNFET simulation

further, the SDEVICE tool is used for initializing appropriate physical and mathematical models across different regions in CNFET.

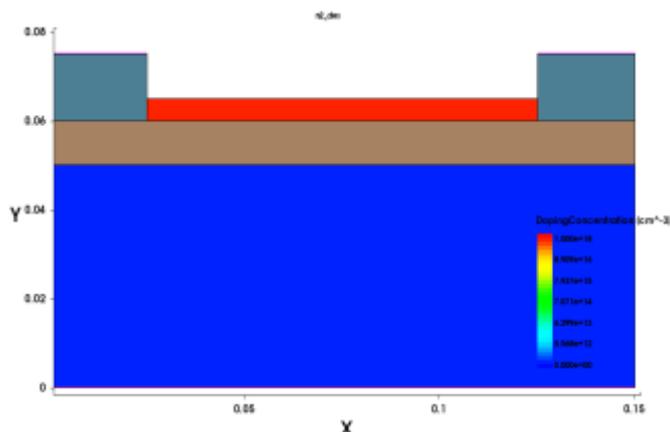


Figure5: Schematic of CNFET structure

B. CNFET Simulation

2D numerical simulation of CNFET is carried out in TCAD to calculate electrical parameters. Simulator makes use of the Poisson’s and drift diffusion formulation discretized over a multidimensional numerical mesh [14]. The Coupled and Quasistationary commands are used to solve a set of equations and to ramp a solution from one boundary condition to another respectively. The Coupled command activates a Newton-like solver over a set of equations includes the Poisson equation, continuity and the different thermal and energy equations [14]. The simulator solved these basic equations using the drift diffusion model evaluating for the potential, hole and electron concentration with appropriate assumptions and calculated the drain current at a specified gate bias. With are very small dimensions of CNFET; some quantum modification items are added to the simulation for results to be closer to the real condition [15, 16]. Optical generation is computed using the transfer matrix method (TMM) which is based on the propagation of plane waves through layered media in CNFET. Shockley–Read–Hall (SRH) and Auger recombination with doping dependence is used to calculate recombination during simulation.

IV. SIMULATION RESULTS

Optical generation in CNFET is activated by illuminating from top using a monochromatic light source whose spectral range varied from 600 nm to 1550 nm. The TMM optical solver requires the use of the complex refractive index model, and various excitation variables, all such excitation variables specified in TMM are listed in table 3

TABLE III. Excitation Variables Used In Optical Generation [17]

Optical Intensity [W/cm ²]	500
Wavelength [nm]	600 - 1550
Theta [deg]	0 (Normal Incidence)
Polarization Angle [deg]	1 (Unpolarized light)

A. Gate Voltage Dependence

Figure 6 presents the plots for the photocurrent under the different bias conditions for CNFET under dark and illumination. It shows that drain current increases with the increase in illumination. This is because with the illumination a forward biasing potential is developed across the SWCNT active layer which increases the channel potential. Also, the photosensitivity of CNFET is highly dependent on the bias voltage, from the plot it can be seen that both photocurrent and dark current are increasing with the increasing bias voltage.

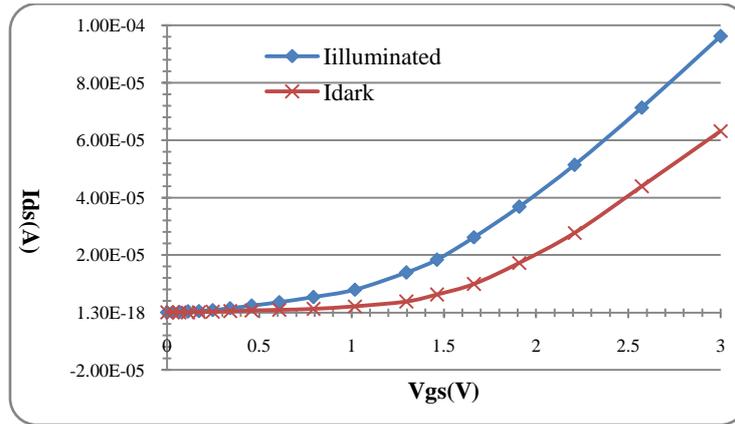


Figure. 6. I_{ds} Vs V_{gs} under dark and illumination. ($L_g=100$ nm and $V_{ds}=0.01$ V)

B. Channel thickness Dependence

Channel thickness is dependent on the diameter of SWCNT as shown in equations 1 and 2. For the CNFET simulation different zig-zag SWCNTs are used and tabulated in the table IV.

TABLE IV Chirality Dependent SWCNT Parameters

Chirality	Diameter (nm)	Band gap (eV)
(13,0)	1	0.497
(17,0)	1.33	0.374

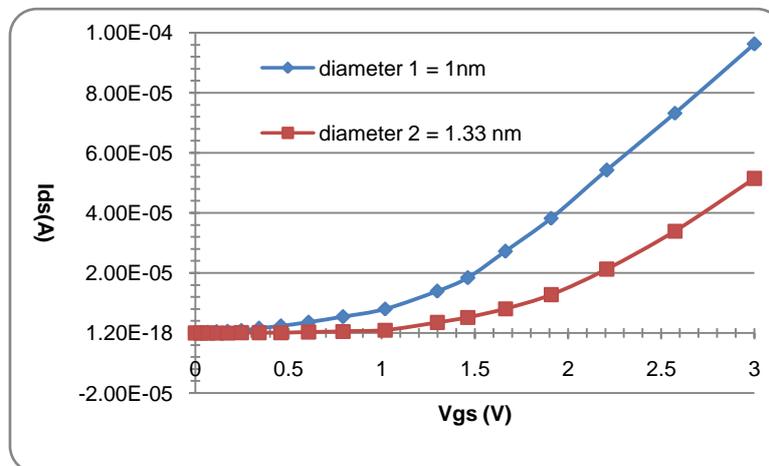


Figure 7 I_{ds} - V_{gs} curve in CNFET with SWCNT (13, 0) and SWCNT (17, 0)

Transfer characteristics between the input voltage V_{gs} and the output drain current I_{ds} are derived for constant $V_{ds} = 0.01$ V. The simulation result for both CNFET's with 100 nm channel length is shown in figure 7. Drain current is increasing with the input voltage V_{gs} . It is observed from the above plot that SWCNT provides the high channel mobility so automatically current increases and linearity is more. But drain current is decreasing with growing tube diameter since in SWCNT the band gap is inversely proportional to its diameter and responsible for reduced carriers across the active channel.

C. Gate Oxide Dependence

The relatively low dielectric oxide such as SiO_2 brings limitations for its use as gate oxide in scaled CNFETs due to high leakage current. With high dielectric gate oxides small thickness deposition is possible and hence allows efficient charge injection into an active channel reducing leakage current. This has further motivated to explore about the integration of high- κ films (~20-30) as gate oxide. The dielectric materials considered for gate oxide during the simulation are listed in the table 5. Gate oxide dielectric material dependent output characteristics of the CNFET are shown in Figure 8, where the thickness of the gate insulator is kept 10 nm.

TABLE V. Gate Oxide Materials Considered in Simulation.

Oxide	Dielectric Constant	Band Gap (eV)
SiO ₂	3.9	9
HfO ₂	25	5.8

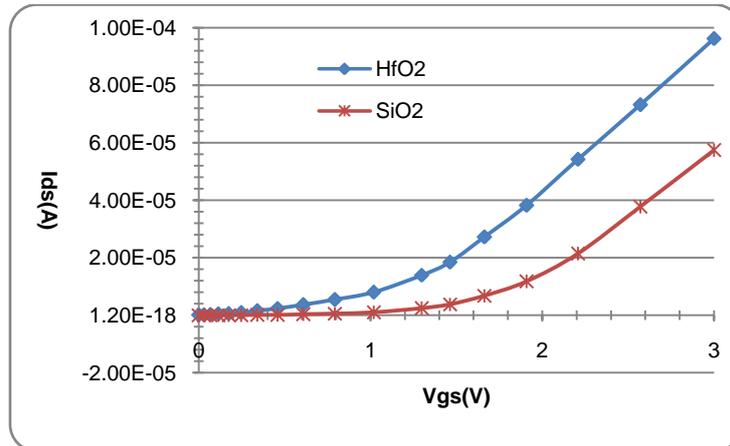


Figure 8. I_{ds}-V_{gs} curves of CNFET for SiO₂ and HfO₂ Physical oxide thickness is kept 10 nm.

The results are obtained for the ramping gate bias V_{gs} from 0 to 5 V, while keeping the drain bias V_{ds} fixed at 0.01 V. Figure 8 shows the I_{ds}-V_{gs} characteristics in CNFET for SiO₂ and HfO₂ gate oxide materials. For the relative dielectric constant of 3.9, the drain current in the CNFET is 10 μA at V_{gs} = 3V. For the high dielectric constant, the drain current increases to 0.388 μA. This rise in the drain current is because of high dielectric HfO₂ oxide. Sheikh Ziauddin Ahmed et al found that with more than 50 % rise in ON current when HfO₂ is used as the gate dielectric [7]. This justifies our results obtained by Sentaurus TCAD simulation software.

For SiO₂ dielectrics, to obtain an electrostatic coupling capacitance approaching the quantum capacitance of an SWCNT, an ultra-thin 1–2 nm SiO₂ layer is required since in SWCNT, the electrostatic coupling capacitance logarithmically depends on thickness. But the thin SiO₂ dielectric causes significant leakage currents, a major transistor scaling trouble.

D. Current Variation at various wavelengths

Figures 9 and 10 depict the variation of current I_{ds} with voltage V_{ds} for the low and high dielectric gate oxide at various wavelengths showing that both models are wavelength insensitive till 500 nm. A prominent decrease in I_{ds} is observed when frequency increases from 1000 nm to 1550 nm because of minority carrier life time.

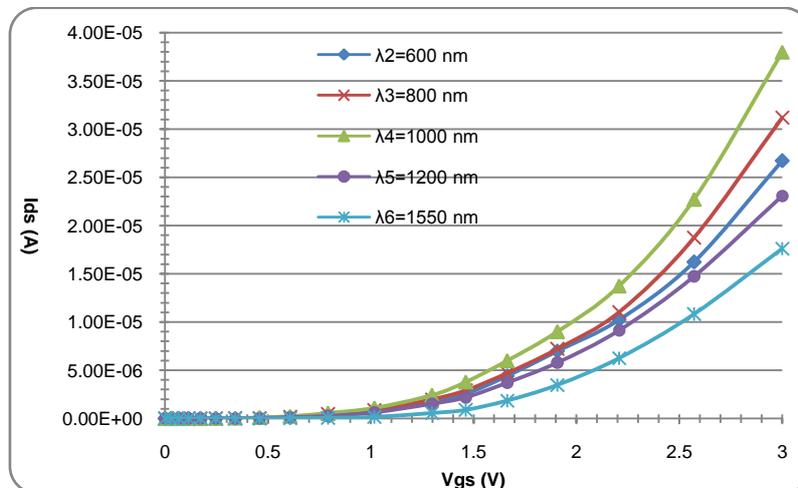


Figure9: Current- Voltage (I_{ds}-V_{gs}) characteristics for different wavelengths at V_{ds}= 0.02 V and gate oxide as SiO₂

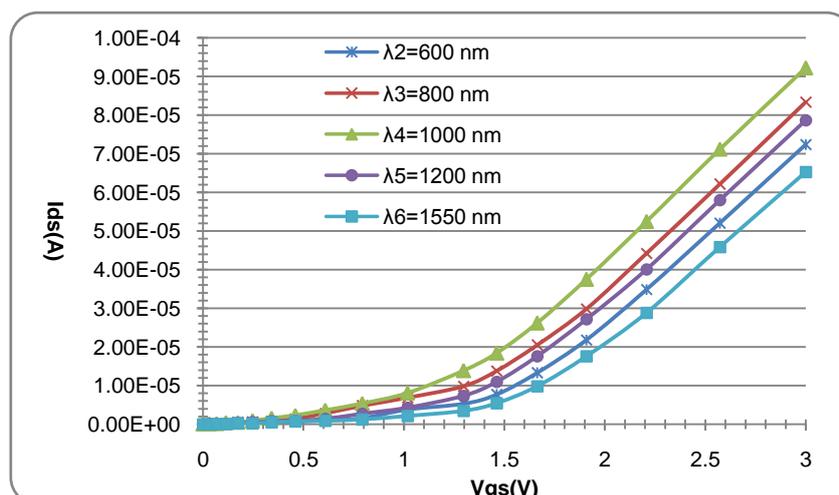


Fig 10: Current- Voltage (I_{ds} - V_{gs}) characteristics for different wavelengths at $V_{ds}= 0.02$ V and gate oxide as HfO_2

F. Verification

Table VI shows the comparison for I_{ds} at various wavelengths for the developed model with the reference model [2]. It shows that the optically generated current for the model developed is comparable to the reference model for the same dimensions and optical illumination.

TABLE VI: Comparison of I_{ds} at different Wavelengths

Wavelength (nm)	I_{ds} (mA) Oxide: SiO_2	I_{ds} (mA) Oxide: HfO_2	I_{ds} (mA) Oxide: SiO_2 [2]
600	0.02672	0.072407	----
1000	0.038	0.0922	0.0452
1200	0.0231	0.0787	0.0448
1550	0.017642	0.065314	0.0400 (at 1400 nm)

V. CONCLUSIONS

This Sentaurus TCAD based simulation model is developed for a CNFET phototransistor. It is observed that the key element for an improved photocurrent to be the superior ability of band engineering in SWCNT incorporated into MOSFET geometries. For CNFET photodetector performance improvement, modifications are done in the phototransistor channels to allocate a wide region for light absorption purpose. Thin SWCNT layer in CNFET acts as an active layer, exhibits an enhanced photo detection capability and is superior to bulk material channels. The charge flow in the SWCNT channel can be strongly controlled by the gate oxide dielectric constant, gate bias and source and drain contact resistance.

Theoretical and TCAD simulation studies have been performed for analyzing the optical performance of back gated CNFET photo transistor with different dielectric oxides (SiO_2 and HfO_2). Through careful optimization of CNFET structure by the use of compact models in Sentaurus TCAD, the impact of the gate oxide dielectric strength on optical generation in CNFET is examined under varied illumination conditions. It has been observed that high dielectric HfO_2 reduces leakage current and significantly improves the output current. CNFET with HfO_2 shows an improved performance compared to SiO_2 with an incremental increase of 142.63 % under same operating conditions. Input as well as output current characteristics of CNFET photodetector show that the drain current is sensitive to SWCNT thickness and biasing. It has been observed that output dark and illuminated drain current decreases for the increasing SWCNT thickness.

Results obtained from the TCAD simulation of CNFET photo detector are encouraging. It is predicted that TCAD simulation might have the possibility to use to model the material SWCNT and thus CNFET phototransistors for analysis and consequently saving the actual production time and cost.

CNFET phototransistor performance can be further improved if the SWCNTs can be densely aligned along the channel, so that light absorption and the mobility of carriers through the film can be maximized. Also investigating more about HfO_2 heterojunction with SWCNT can further optimize trap densities in the oxide layer and improve the photo absorbance of CNFET phototransistor.

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