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Review of Comparison of various Sub threshold Srams at 65nm CMOS Technology

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ABSTRACT
An SRAM (Static Random-Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs, and to replace DRAM(Dynamic Random-Access Memory) in systems that require very low power consumption. This paper is evaluating different design of SRAM performance in terms of Size, Speed, and Cell type, Leakage current and minimum voltage at 65nm CMOS technology.
KEYWORDS: 65nm CMOS technology, size, speed, cell type, leakage current, minimum voltage.

I. INTRODUCTION

1. Introduction

Memories have always been an area of great interest and research. Static Random-Access Memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications.The SRAM cell utilizes a conventional six-transistor design and has an area of $0.1um^2$, breaking the previous SRAM scaling barriers. The new technology provides a function for switching dynamically, with a low power overhead, between active operation, in which the CPU core performs read and write operations of the embedded SRAM, and the standby mode, in which the stored data is retained.SRAM memory from ON Semiconductor consumes the least power, and is specifically designed and qualified for implantable medical applications. [3] In patients with pacemakers, these SRAMs remember the last day's ECG signals, which facilitates much more accurate clinical diagnoses when needed and provides the best possible patient outcomes.

II. 6T SRAM OPERATION

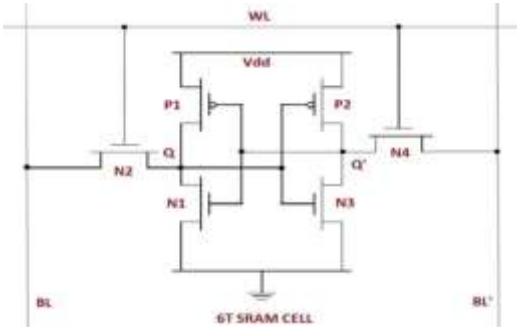

Figure1. 6T SRAM

There are three conditions of operation for SRAM cell: standby, read and write modes.
Standby:The WL (word line) is lowered to 0V, turning the both N-MOS access transistors off. In this situation the CMOS inverters are in complementary state. When P-MOS (left inverter) is turned on, the voltage at node Q is Vdd and the P-MOS of the right inverter is turned off, Q' is 0V.
Reading: '0' is stored in the cell (Q=0)

- When WL is at 0V, both PA (access transistors) are off

- Pre-charge both bit-lines (BL and BL') high
- WL (word line) to high.
- 'Q=0, Q'=1' is saved, WL=High causes N2 to pass 0V to N3/P2, VDD to N1/P1.
- Current flows from P2 to N4, so charging the BL' bit-line voltage.
- Current flows from N3 to N1, so discharging the BL bit-line voltage. Voltage difference of BL to BL' of 50-100mV is sensed at the sense amplifier.

'1' is stored in cell (Q=1)

- When WL is at 0V, both PA (access transistors) are off
- Pre-charge both bit-lines high.
- WL will go high.
- "Q=1, Q'=0" is saved, WL=High causes N2 to pass Vdd to N3/P2, 0v to N1/P1.
- Current flows from N3 to N3, so discharging the BL' bit-line voltage.
- Current flows from P1 to N2, so charging the BL bit line voltage. Voltage difference of BL to BL' of 50-100mV is sensed at the sense amplifier.

Writing: '1' is updated content in the cell, initially '0' is stored.

- When WL is at 0V, both access transistors are off
- One bit-line is raised to high (Q=BL=Vdd), the other is lowered to 0V (Q'=BL'=0V)
- WL (word line) to high
- Drain terminal of N2 (BL) goes to 0 to (Vdd-Vt), and source terminal of N4 (BL') goes to Vdd to 0V.
- '1' is stored on Q.

'0' is updated content in the cell, initially '1' is stored.

- When WL is at 0V, both access transistors are off
- One-bit line is raised to high (BL=Vdd), the other is lowered to ground (BL'=0V)
- WL (word line) to high
- Drain terminal of N4 (BL) goes to 0 to (Vdd-Vt)
- Source terminal of N2 (BL') goes to Vdd to 0, cell stores a "0" on Q.

III. SURVEYED DESIGNS

Dake Liu and Christer Svensson, 1993 has realized Trading speed for low power by choice of supply and threshold voltages. The author of this paper has presentedthe trading of speed for low power consumption in CMOS VLSI by using the supply voltage and the threshold voltage as variables has been investigated. It has been shown that it is desirable to minimize the supply voltage for minimizing the power consumption.

B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, 2008 has presented a variation-tolerant sub-200 mV 6-T sub-threshold SRAM. The author of this paper has presented a deep sub-threshold 6-T SRAM, which was fabricated in an industrial 0.13 m CMOS technology. [1] The author has used detailed simulations to explore the challenges of ultra-low-voltage memory design with a specific emphasis on the implications of variability. The author has proposed a single-ended 6-T SRAM design with a gated-feedback write-assist that remains robust deep in the sub-threshold regime. Measurements of a test chip has shown that the proposed memory architecture functions from 1.2 V down to 193 mV and provides a 36% improvement in energy consumption over the previously has been proposed multiplexer-based sub threshold SRAM designs while using only half the area.

N. Verma and A. P. Chandrakasan, 2008 has presented a 255 kb 65 nm 8T subthreshold SRAM applying sense-amplifier overabundance.Scaling the supply voltage of SRAMs highly minimizes their effective and dissipated power, a domineering section of the total power in ICs. [2] Hence, energy strained applications, where performance requirements are secondary, uses significantly from an SRAM that attemptwrite and read functionality at the lowest available voltage. However, bit-cells and architectures attaining high density commonly fail to operate at low voltages. This paper has been described a high-density SRAM in 65 nm CMOS that performs an 8T bit-cell to attain a minimum operating voltage of 349 mV.

M. Sharifkhani and M. Sachdev, 2007 has presented the Segmented virtual ground architecture for low-power embedded SRAM.A new design to cut down the power dissipation of static random-access memories is conferred. It has been shown that using segmented virtual grounding, it is possible to reduce both dynamic and static power dissipation. [3] The saturated power of the cells has cut down by reducing the voltage drop over a cell. The dynamic power consumption is scaled down by eliminating the power dissipation due to the discharge of the non-desired bit-lines.

Manoj Sachdev, 2017 has presented a 288-mV, 3.33-MHz, 6T SRAM withpMOS Access Transistors in 65-nm CMOS Technology. This paper has been presented a 6-Tbitcell SRAM with pMOS access transistor. ApplyingpMOS access transistor performs in lower zero-level degradation (ZLD) and, hence, higher read stability. [4] The access transistor connected to the internal node equity*V*DD acts a stabilizer and counter balances the effect of ZLD. In order to develop the writability, wordline (WL) boosting has been exploited.

Massimo Alioto,2012 has presented the Ultra-Low Power VLSI Circuit Design Demystified.In this paper, the author has detailed of the art in ultra-low power (ULP) VLSI design is given within a unitary framework for the first time [5]. A few general principles are first received to gain an insight into the design issues and the access that are specific to ULP systems, as well as to better explained the challenges that have to be faced in the computable future.

Fran J. List, and Jan Loshtroh, 1987 has conferred Static-Noise Margin Analysis of MOS SRAM Cells. The stability of both resistor-load (R-load) and full-(2MOS SRAM cells has been considered analytically as well as by simulation. Explicit analytic expressions for the static-noise margin (SNM) as a function of device parameters and supply voltage has been derived. [6] The author has derived the expressions that are useful in checked the effect of parameter changes on the stability as well as in reducing the design of SRAM cells.

Nahid Rahman, B. P. Singh, 2013 has presented Static-Noise-Margin Analysis of Conventional 6T SRAM Cell at 45nm Technology. Static random-access memory is a type of volatile memory to store binary logic '1' and '0'. [8] The SRAM sizing has been reduced due to the increase density of SRAM in System-On-Chip (SoC) and other integrated devices, which works on lower supply voltage. This leads to appreciable amount of power saving, but the stability and performance of the SRAM circuit is also being concerned due to the scaling of supply voltage.

Table1. Comparison of Performance parameters of Different SRAM Cell

Design	CMOS technology	Size (Kb)	Cell type	I (leakage) (nA/b)	Speed (MHz)	V(min) (mV)
JSSC13	65	2	9T	N.A	1.2	220
JSSSC08	65	256	8T	0.024	0.025	350
JSSC16	65	35	8T	0.034	2	200
JSSC13	65	32	7T	N.A	8.5	260
JSSC08	130	2	6T	119	0.45	210

IV. CONCLUSION

A comprehensive survey has been completed for different design of Static Random-Access Memory. These layouts are well approved for different low power applications. Different techniques to reduce the power consumption has been advanced and it can be preferred for low power and high-speed applications.

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