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# Design Of Logic Circuits Using Adiabatic Hybrid Mtj-Cmos

Dr.M.Shyam sundar
*Assoc.prof Kamala Institute of Technology and Science, Huzurabad, Karimnagar*
*Corresponding Author: Dr.M.Shyam Sundar*

***ABSTRACT**: Low-power designs are a need with the increasing demand of compact devices which are battery worked. In a significant number of such devices the operational speed isn't as critical as battery life. Logic-in-memory structures using nano-devices and adiabatic designs are two techniques to decrease the static and dynamic power consumption separately. Magnetic tunnel junction (MTJ) is an emerging technology which has numerous focal points when utilized as a part of logic-in-memory structures in conjunction with CMOS. In this paper, we introduce a novel adiabatic hybrid MTJ/CMOS structure which is utilized to plan AND/NAND, XOR/XNOR and 1-bit full adder circuits. We simulate the designs using HSPICE with 32nm CMOS technology and contrasted it and a non-adiabatic hybrid MTJ/CMOS circuits. The proposed adiabatic MTJ/CMOS full adder configuration has more than 7 times lower power consumption contrasted with the past MTJ/CMOS full adder.*

***Keywords:** Magnetic tunnel junction, adiabatic, low power CMOS*

## I. INTRODUCTION

In the last decade, internet of thing (IoT) devices, portable electronics, for example, smartphones, tablets and sensors has increased significantly. The greater part of these devices are battery worked and consequently power consumption (battery-life) has moved toward becoming a critical design constraint. Consequently, researchers set out to find new techniques for designing low-power electronics [1]. A technique for designing low power electronics that decreases the leakage power consumption is to utilize non-conventional CMOS devices and using emerging nanotechnologies. Some new emerging technologies are extremely suitable to be used in low power applications [2]. Another technique for reducing the dynamic power consumption is to recoup the stored energy in the load capacitor instead of dissipating it as heat. This approach which works based on energy recovery is known as adiabatic (reversible) circuit design [3].

Also, ultra-low power architectures can be acknowledged by logic-in-memory (LiM) paradigm, where memory elements are dispersed over logic circuits [10-11]. Magnetic tunnel junction (MTJ) is a nonvolatile memory that has short access time, little measurements and compatible with CMOS technology [12]. Along these lines, it is most suited to use in logic-in-memory architectures. LiM structures using MTJs are extremely suitable to low power designs, in light of the fact that the static power dissipation is just about zero in these circuits.

Then again, in present day integrated circuits and systems with high switching activity, dynamic power plays a huge part in power consumption. Dynamic power dissipation is expected to charging and discharging of load capacitors during output switching. Adiabatic circuits are a group of circuits which diminishes the dynamic power consumption by methods for energy recovery to the supply voltage. In adiabatic circuits a multiphase clock controls the charging and discharging of the load capacitor. There are two sorts of adiabatic circuits, fully adiabatic and quasi adiabatic circuits. In fully adiabatic circuit the leakage power through the switches is the only power loss, while in quasi adiabatic circuits some non-adiabatic power losses exist [13,14].

In this paper, we exhibit Spin-MTJ based nonvolatile adiabatic family of circuits. To the best of our insight, this think about is the first on nonvolatile adiabatic circuits. The remainder of the paper is sorted out as follows: a short survey of MTJ devices and adiabatic circuits is introduced in Section II. The proposed circuits are portrayed and investigated in Section III. Finally Section IV concludes the paper.

## II. BACKGROUND

**Magnetic tunnel junction review:**

Magnetic tunnel junction (MTJ) consists of two ferromagnetic (FM) layers (one of the layers is fixed and the other one is free) and an oxide barrier layer sandwiched between these two layers. The oxide barrier has the ability to store data more than ten years which is verified by Time-Dependent Dielectric Breakdown (TDDB) experimental measurements [15,16]. Two possible configurations (parallel and anti parallel) can be materialized according to the FM layers alignment. Based on these two configurations, an MTJ shows low resistance (RP) or high resistance (RAP) characteristics [17]. Thus, we can use these characteristics to implement LiM designs.

Three main methods have been proposed for switching MTJ configuration: Field Induced Magnetization Switching (FIMS), Thermally Assisted Switching (TAS) and Spin Torque Transfer (STT). The most promising method is STT which was proposed as an alternative for the other two methods. STT requires only one bi-directional low switching current. The states of the MTJ are switched when the current of MTJ (IMTJ) becomes higher than a critical current (IC) [18]. FIMS was the conventional approach for switching MTJ states; RAP and RP, which were based on applying a magnetic field. This method suffers from high power consumption, poor selectivity, and poor scalability due to its high switching currents.[22]

**Adiabatic logic:** Adiabatic logic is one of the low-power circuit design techniques at cost of slower speed of operation. The general schematic of an adiabatic technique is appeared in Figure 1. In adiabatic circuits the load capacitance is charged by a constant current source not at all like conventional CMOS where, the load capacitance is charged by a constant voltage source. Adiabatic logic reduces the overall power consumption of the circuit by utilizing a clocked AC power to charge the load capacitor and recovers vitality from the charged capacitor in a slow manner to eliminate dynamic power dissipation [19].

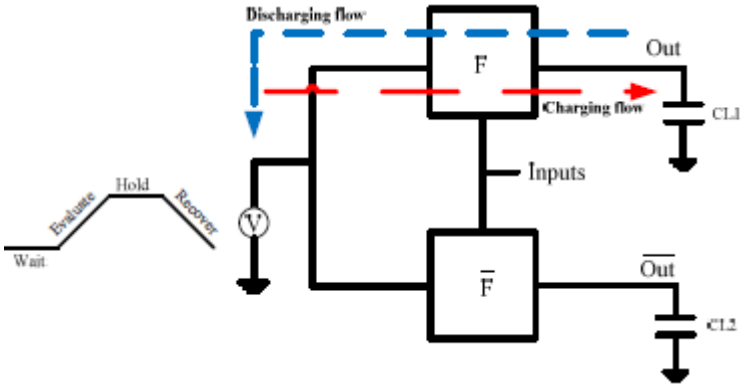


**Fig1:** adiabatic charging and discharging

The energy dissipated in an adiabatic circuit can be calculated based on the following equation [3]

$$E_{diss} = RC/T(CV_{dd}^2) \qquad \text{----------} \qquad (1)$$

Where, C is the load capacitor, T is the capacitor charging time, and VDD is the full swing of the power clock. In order to have less power consumption than conventional CMOS, adiabatic circuits have a charging time (T) that is greater than 2RC.

**Proposed design and evaluation:**

In this section, we propose MTJ-based adiabatic circuits family. To the best of our insight this is the primary attempt to design adiabatic magnetic circuits. MTJ-based circuits are generally composed of three parts as in Figure 2. The initial segment is a written work circuit, which is utilized for programing the memory elements. The second part constitutes of STT-MRAM cells and CMOS logic tree which as a logic control block. Finally, the last part is a sense amplifier (SA) that evaluates the output logic results.

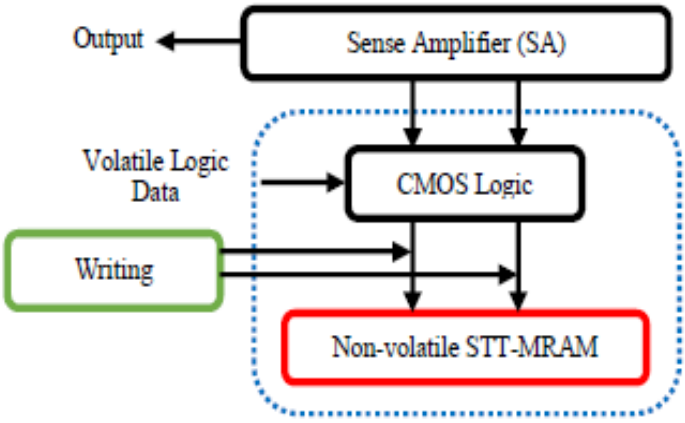


**Fig.2.** structure of a MTJ based circuit

A general perspective of the proposed adiabatic MTJ-based circuit family is in Figure 3. The difference between the presented circuits and MTJ-based circuits in the literature [12] is in the SA structure. To charge and discharge the outputs, a clocked AC power supply is utilized which has four phases (wait, evaluate, hold, and recover) as in Figure 1. Also, we utilize a N-MOS transistor to have an equal charge in the wait phase. In this way, the discharge signal is VDD when the circuit is in the wait phase.[22]

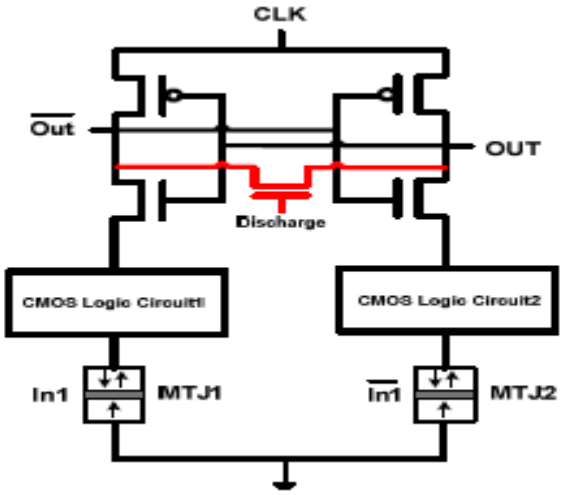


**Fig.3:** General schematic of the proposed adiaatic hybrid MTJ/CMOS design.

The initial states of MTJ and MTJ2 are anti parallel and parallel respectively. In the proposed method, we eliminated two P-FETs and an N-FET from the circuits presented in [12]. In this paper, adiabatic MTJ-based logic gates and arithmetic circuits including AND/NAND, XOR/XNOR gates and a full adder cell are presented in the next subsections.

**Logic Gates (AND/NAND, XOR/XNOR):**

The schematic design of the gate is shown in Figure 4. When the CLK is within the wait phase, each AND moreover as NAND outputs are zero. Assume that the input pattern is " 01" for " AB" then, T5 are going to be off and MTJ1 and MTJ2 are going to be in parallel and antiparallel states, severally. With this input pattern, the left path is cut off and therefore the AND output are going to be discharged to the ground and consequently the NAND output can charged to VDD in the evaluate phase. The outputs can stay constant within the hold phase whereas within the recovery phase, the NAND output can be discharged to the CLK supply power. Since T1 and T2 cannot discharge the outputs utterly to zero, within the next wait part the discharge signal are going to be VDD to share the outputs voltages and each outputs have constant quantity of voltage.

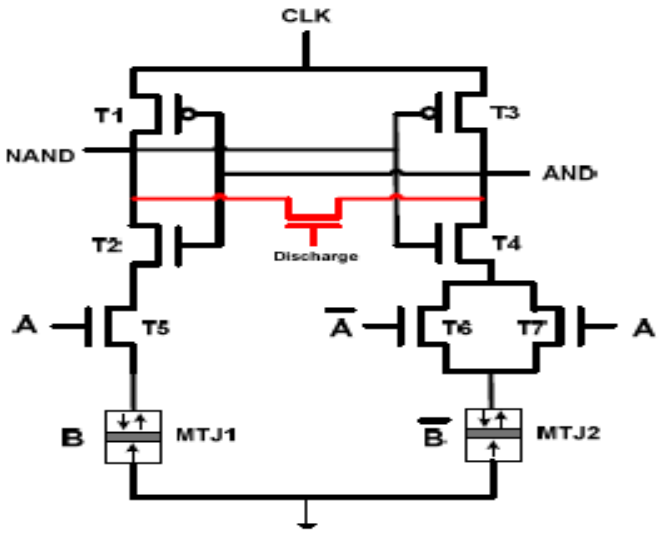


**Fig.4** Proposed adiabatic hybrid MTJ/CMOS AND/NAND.

In the following we elaborate more on the functionality of the proposed XOR as in Figure 5. Consider that the input pattern is " 00" for " AB" and therefore the initial states of MTJ1 and MTJ2 are anti parallel and parallel, respectively. At the wait phase, the recollections memories programmed since the voltage level of the clock is zero. Thus, the states of MTJ1 and MTJ2 stay at the previous states as a result of the voltage of input B wasn't modified. At the evaluate phase the writing circuit is disconnected from the main circuit and therefore the voltage level starts to extend. With this input pattern, T2 and T3 are ON and MTJ2 has a lower resistance than MTJ1. Since the left path has additional resistance (because of the anti parallel state of MTJ1), the XNOR output are going to be charged and therefore the XOR output will remain zero within the evaluation phase. The voltage level of the XOR and XNOR outputs can stay at zero and VDD within the hold phase. Finally, within the recovery phase the outputs are going to be discharged and recovered to the CLK. Now, contemplate the input patterns visit " 01" from " 00" within the wait part, therefore the states of MTJ1 and MTJ2 can modification from antiparallel to parallel and vice versa, severally. T2 and T3 are going to be ON and MTJ1 can have lower resistance than MTJ2. consequently, the resistance value of the right path are going to be higher than the left path, and the XOR output are going to be charged throughout the evaluate phase. When the inputs value is " 11" , the states of MTJs can remain an equivalent. In this pattern, T1 and T4 are ON and since MTJ2 has additional resistance, the XOR output can stay 0V and XNOR are going to be charged within the evaluate phase. Throughout the hold phase, the outputs won't be modified and within the recovery phase the XOR output will follow the CLK voltage to zero.

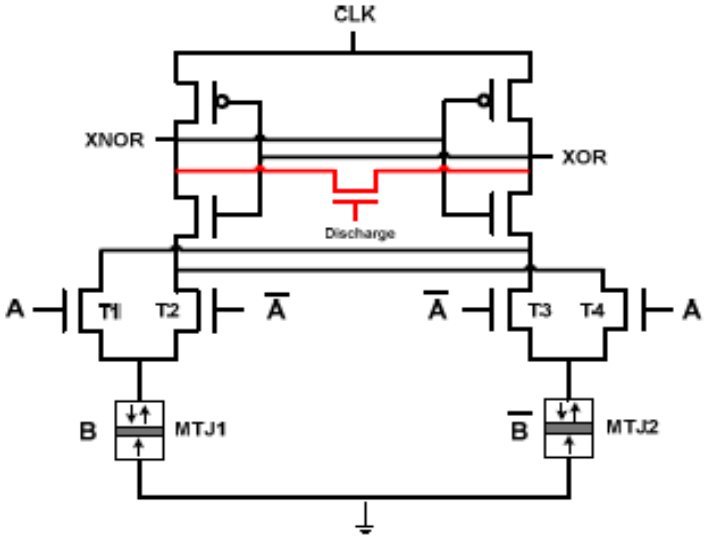


**Fig.5**.Proposed adiabatic hybrid MTJ/CMOS XOR/XNOR

**Full adder cell:**

Figure 6 depicts a schematic of the proposed full adder cell. The initial state of the MTJ1 and MTJ3 is anti parallel and the initial state of the MTJ2 and MTJ4 is parallel. The principle of operation of this circuit is similar to the proposed XOR circuit but with a different output. The Sum and Carry out of the adder are given in equations 2--5.

$SUM = ABC + AB'C'+A'BC'+A'B'C$ ---------- (2)
$SUM' = ABC'+AB'C+A'BC+A'B'C'$ ---------- *(3)*
$C_{out} = AB+AC+BC$ ---------- *(4)*
$C_{out}' = A'B'+A'C'+B'C'$ ---------- *(5)*

For example, when the inputs pattern is " 001" for " ABC" , the *SUM '* output will be zero via the T2, T8 and MTJ2 and consequently the Sum will be charged in the evaluate phase. Also, Cout will be zero through the path of T11 and MTJ4.

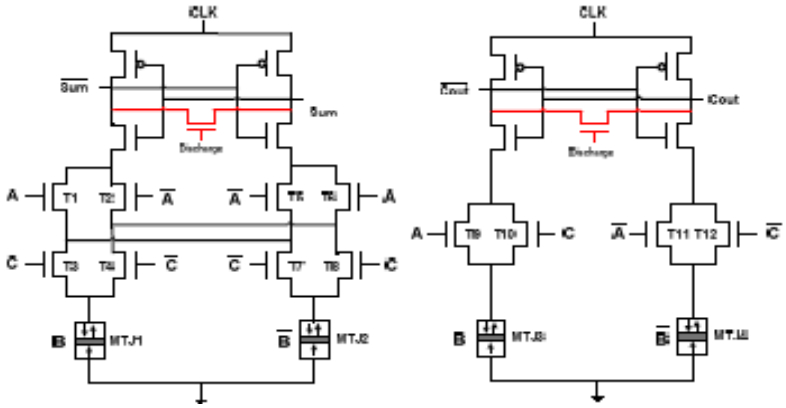


**Fig.6:** Proposed adiabatic hybrid MTJ/CMOS full adder design.

**Designs Evaluation and Comparison:**

The proposed design are simulated and compared at with the MTJ/CMOS outline in [12] regarding power utilization. simulations are led utilizing the HSPICE circuit test system with 32nm technology for CMOS transistors [20] and the spice MTJ model demonstrate introduced in [21] for MTJ devices. Figure 7 demonstrates the transient response of the proposed XOR design when the input B is VDD. It confirms the right operation of our design. The comparison consequences of our proposed plans and the design in [12] are delineated in Figure 8. The diagrams recommend that the proposed adiabatic hybrid MTJ/CMOS XOR, AND, and the full adder designs have very nearly 13, 6 and 7 times lower power consumption compared with the designs introduced in [12].

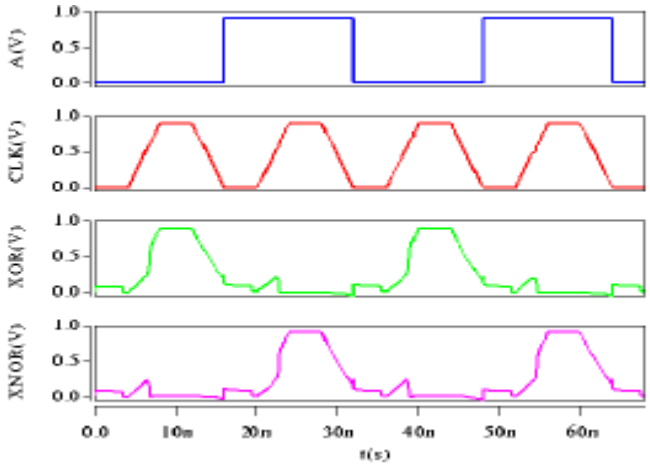


**Fig. 7.** Transient response of the proposed adiabatic hybrid MTJ/CMOS full adder circuit. Here it is assumed that the input " B" is logic " 1" and stored in MTJs.

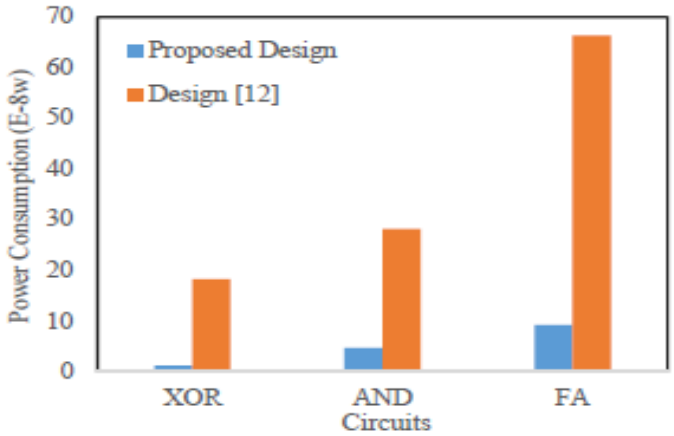


**Fig. 9.** Power consumption of the proposed designs and designs [12].

## III. CONCLUSION

Logic-in-Memory (LiM) structures that utilization magnetic devices furthermore, adiabatic designs are two proficient ways to deal with realize low power designs. Another structure for designing adiabatic hybrid MTJ-CMOS circuits is displayed in this paper. We have executed AND/NAND, XOR/XNOR, and full adder circuits with this structure. Designs are simulated and contrasted and best in class. We utilized Synopsys HSPICE simulator with 32 nm technology records to assess our designs. The outcomes appear that the proposed adiabatic MTJ-CMOS designs have lower power utilization contrasted with cutting edge, to such an extent that the proposed XOR, AND, and full adder have just about 13, 6, and 7 times lower power utilization individually contrasted with state of the art.

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