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A New Symmetric and Asymmetric type of Multilevel Inverter with reduced number of Switch and Capacitor

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Abstract:*In this paper, a novel multilevel inverter topology which can be operated in both symmetrical and asymmetrical configurationshasbeenproposed.Inordertoproduceallstepsof voltage at output, four different algorithms are proposed to find the value of DC sources. The proposed topology reduce switch count, gate driver circuits, total voltage blocking capability and isolated DC voltage sources which leads to reduction in installation space and cost. For switching purpose multiple carrier PWM strategy has been used. Simulation results have been presented for 9-level, 17-level and 53-level operation of proposed inverter using MATLAB/SIMULINK software and the feasibility of topology has been validatedexperimentally.*

Keywords: Total harmonic distortion, Multiple carrier PWM strategy, Total voltage blocking capability.

I. INTRODUCTION

In the modern era, the multilevel inverters are receiving attention in the field of power electronics because of their considerable advantages such as high power quality, lower total harmonic distortion (THD), better electromagnetic consistence, lower *dv/dt*, and lower switching losses [1–6]. Since its invention the demand is growing steeply in the area of AC motor drives, uninterruptible power supplies, high- voltage DC power transmission, flexible AC transmission systems, static var compensators, active filters, electric and hybrid electric vehicles and integration and utilization of renewable energy sources.

The conventional multilevel inverter (MLI) topologies like neutral point clamped inverter (NPC) and flying capacitor inverter (FC) uses a single common source where as cascaded multilevel inverter topology uses multiple isolated dc sources. Single DC source is used in diode clamped technology but the requirement of clamping diodes is very large. In flying capacitor topology, capacitors are placed in place of clamping diodes. Hence, the control becomes intricate along with increase in the overall size of the inverter [7-11]. Thecascaded multilevel inverter (CMLI) topology is favored because of its modular nature, flexibility and convenient to protract. H- bridge is the basic building block in Cascaded multilevel inverters. Each H-bridge unit is having four unidirectional switches besides a DC source to produce two different voltage levels along with a zero level. The conventional topology of CMLI consists of number of cascaded H-bridge units as instructed by the number of voltage levels that are neededatthe output. Therefore, the number of isolated voltage sources, controlled switches and other circuit components increases with the voltage steps, which raises the control complexity, size, expense of the system and decreases reliability.

Number of voltage steps produced at the output can be raised by using same circuit components by proper selection of the values of the DC voltage sources. In The CMLI topology, if the value of all the DC sources are equal then it is called symmetric and asymmetrical otherwise. The two prominent asymmetrical algorithms which have been broadly used in the conventional CMLI structure are binary and ternary (magnitudes are in geometric progression of 2 and 3 respectively). The number of voltage steps produced by n basic H-bridge modules is givenby,

$N_{level} = 2^{n+1} - 1$, for binary progression

$N_{level} = 3^{n}$, for ternary progression

The above expressions affirming that more levels can be produced at the output without raising the circuit components by suitable selection of the value of the input DC sources. Still, the main drawback of CMLI is that it uses large number of switches and DC sources. Thus, various new topologies [12-16], with

a goal to lower the number of circuit components needed have been recited inliterature.
The key features of the proposed topology are:

- A new MLI topology with reduced number of switches and isolated DC sources isproposed.
- Rapid increase in the levels of output voltage just by addition of few switches in asymmetrical configuration.
- Less number of controlled switches and corresponding gate driver circuits thereby making the circuit lesscomplex.

Thispaperisorganizedasfollows.SectionIIdiscussesthe proposed topology. Section III describes modulation scheme employed. Section IV compares robustness of proposed topology.SectionVvalidatesthetopologythroughsimulations and experiments. Finally, concluding remarks are stated in sectionVI.

II. PROPOSEDTOPOLOGY

The basic unit for the proposed symmetric multilevel inverter is shown in Fig. 1. In this circuit, when the switch S is turned off, the current flows through the diode, but when the switch S is turned on, the diode will get reverse biased and the current flows from capacitor and switch S which are connected in series. Thus by utilizing this technique the output voltage can be controlled. The proposed topology consists of two sections firstly level generator which is responsible forthe generation of stepped voltage waveform and secondly the polarity generator which is responsible for generating the polarity of the output voltage. The switching states of basic unit are given in TableI.

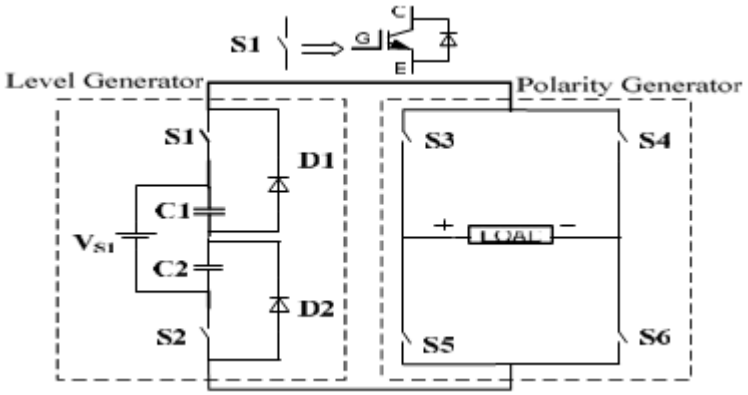


Fig. 1. Basic unit of proposed topology

TABLE I. SWITCHING STATES OF BASIC UNIT

State	'ON' state switches	Conducting diodes	Corresponding output voltage
1	S_1,S_2,S_3,S_6	-	V_S
2	S_2,S_3,S_6	D_1	$V_S/2$
3	S_3,S_4	-	0
4	S_1,S_4,S_5	D_2	$-V_S/2$
5	S_1,S_2,S_4,S_5	-	$-V_S$

The generalization of proposed topology is given in Fig.3 In topology with 'n' basic units,

$N_{source}=n$ (1)

$N_{IGBT}=2n+4$ (2)

$N_{diode}=2n$ (3)

$N_{capacitor}=2n$ (4)

Total blocking voltage across all the switches in level generator = $V_{s1}+V_{s2}+V_{s3}+---+V_{sn}$.

A. Symmetrical configuration:

Proposed symmetrical (Vs1=Vs2=100v) 9-level topology along with its switching states are presented in Fig. 2 and Table II respectively.

Number of levels in the output voltage,

$N_{level}=4n+1$ (5)

Using (2) and (5) we can get,

$N_{level}=2N_{IGBT}-7$ (6)

Total blocking voltage across all the switches in level generator =n ×V_s.
Where 'n' is the number of the basic units=Number of DC voltage sources.

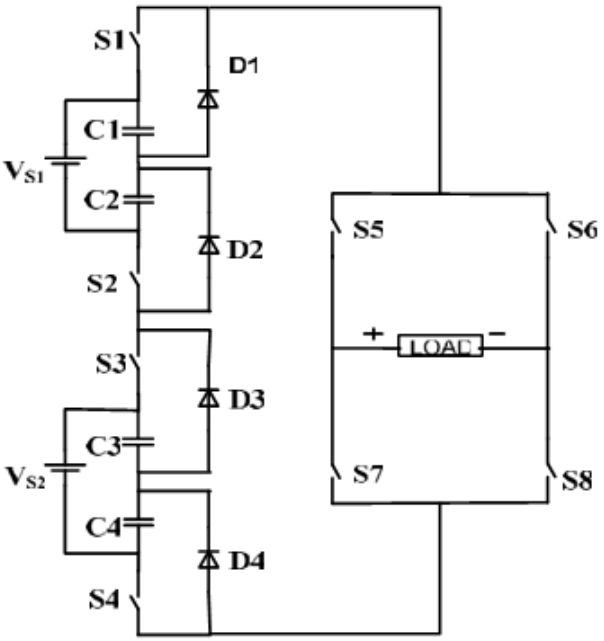


Fig. 2. Configuration of proposed topology

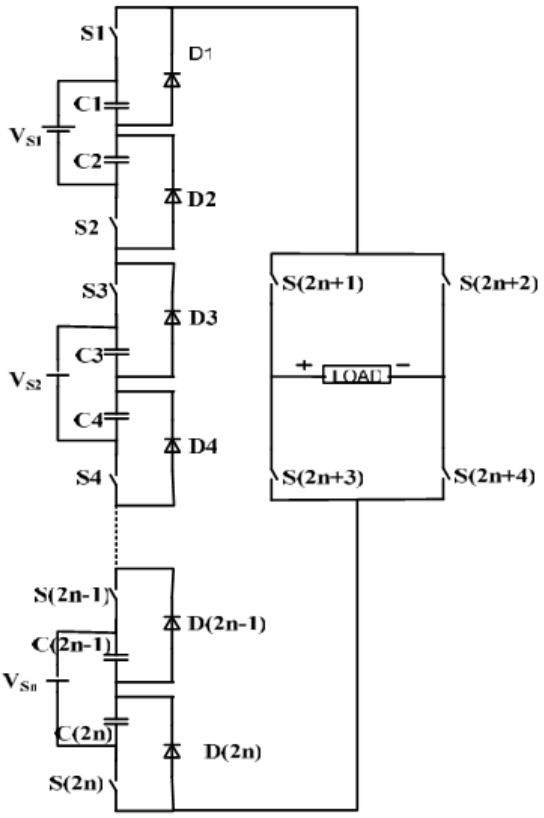


Fig. 3. Generalized configuration of proposed topology

TABLE II. SWITCHING STATES OF PROPOSED TOPOLOGY FOR 9-LEVEL OUTPUT (V_{S1}= V_{S2}=100)

State	'ON' state switches	Conducting diodes	output voltage
1	S_1,S_2,S_3,S_4,S_5,S_8	-	200
2	S_1,S_2,S_4,S_5,S_8	D_3	150
3	S_1,S_2,S_5,S_8	D_3,D_4	100
4	S_2,S_5,S_8	D_1,D_3,D_4	50
5	S_5,S_6	-	0
6	S_1,S_6,S_7	D_2,D_3,D_4	-50
7	S_1,S_2,S_6,S_7	D_3,D_4	-100
8	S_1,S_2,S_3,S_6,S_7	D_4	-150
9	S_1,S_2,S_3,S_4,S_6,S_7	-	-200

B. Asymmetricalconfiguration:

As compared with the symmetrical configuration asymmetrical configuration gives more number of levels for same device count. Fig. 2 shows the structure of the proposed asymmetric inverter where $V_{s1}\neq V_{s2}$. Four different algorithms are given in Table IV to find out the magnitudes of DC voltage sources for the proposedtopology.

In a topology with 'n' units,

1). Ternary progression :

$$N_{IGBT}=2n+4 \quad (7)$$

$$N_{level}=2(3^n)-1 \quad (8)$$

Using (7) and (8) we can get,

$$N_{level}=2\{3^{[(N_{IGBT}-4)/2]}\}-1 \quad (9)$$

2). Binary progression :

$$N_{IGBT}=2n+4 \quad (10)$$

$$N_{level}=4(2^n)-3 \quad (11)$$

Using (10) and (11) we can get,

$$N_{level}=4\{2^{[(N_{IGBT}-4)/2]}\}-3 \quad (12)$$

From the equations (8) and (11) it is clear that ternary progression produces more levels compared to others. So in this paper ternary progression is used for asymmetrical configuration and 17-level and 53-level outputs are obtained with 2 and 3 basic units respectively.

Total blocking capability of all switches in the level generator of asymmetrical configuration=$V_{S1}+V_{S2}+\cdots+V_{Sn}$.

From equation (8) it is clear that number of levels in output voltage increase significantly with number of units.

III. MODULATIONSCHEME

Multi-carrier PWM strategy has been used with triangular wave as carrier signal with frequency of 100 Hz, whereas sinusoidal wave as reference signal with frequency 50 Hz. In multi carrier PWM scheme [17], carrier signals are compared with reference signal and pulses so obtained are utilized for switching of devices corresponding to their respective voltage levels. In Fig. 4 the modulation scheme for 9-level inverterhas been presented. As the Number of levels increases corresponding carriers also increases and the increment is directly proportional. The switching signals are gotten from this aggregated signal by comparison of the signal with desired level and the output is fed to the switches corresponding to the level using the lookup table, given in TableII.

TABLE III. SWITCHING STATES OF PROPOSED TOPOLOGY FOR 17-LEVEL OUTPUT (V_{S1}= 50, V_{S2}=150)

State	'ON' state switches	Conducting diodes	Output voltage
1	S_1,S_2,S_3,S_4,S_5,S_8	-	200
2	S_2,S_3,S_4,S_5,S_8	D_1	175
3	S_3,S_4,S_5,S_8	D_1,D_2	150
4	S_1,S_2,S_4,S_5,S_8	D_3	125
5	S_2,S_4,S_5,S_8	D_1,D_3	100
6	S_4,S_5,S_8	D_1,D_2,D_3	75
7	S_1,S_2,S_5,S_8	D_3,D_4	50
8	S_2,S_5,S_8	D_1,D_3,D_4	25
9	S_5,S_6	-	0
10	S_1,S_6,S_7	D_2,D_3,D_4	-25
11	S_1,S_2,S_6,S_7	D_3,D_4	-50
12	S_3,S_6,S_7	D_1,D_2,D_4	-75
13	S_1,S_3,S_6,S_7	D_2,D_4	-100
14	S_1,S_2S_3,S_6,S_7	D_4	-125
15	S_3,S_4,S_6,S_7	D_1,D_2	-150
16	S_1,S_3,S_4,S_6,S_7	D_2	-175
17	S_1,S_2,S_3,S_4,S_6,S_7	-	-200

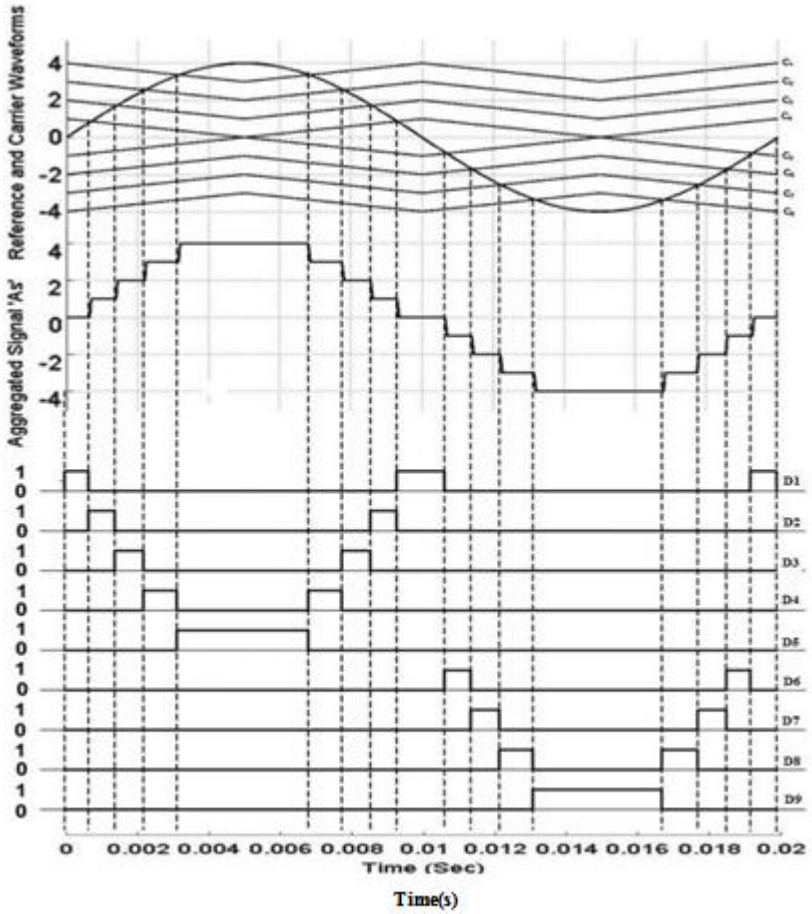


Fig. 4. Waveforms corresponding to proposed modulation scheme

TABLE IV. DIFFERENT ALGORITHMS FOR PROPOSED MLI

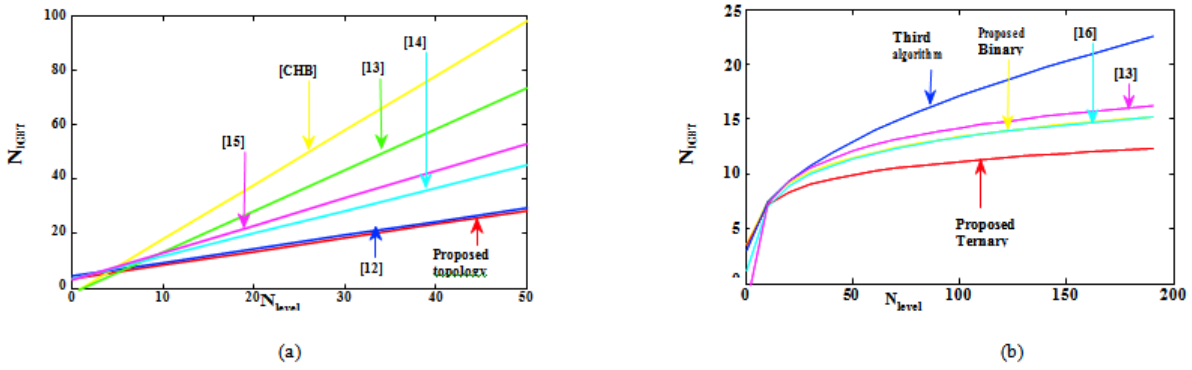
Algorithm	Values of DC sources	Number of output levels	Configuration
First	$V_{s1}=V_{s2}=\cdots=V_{sn}=V_s$	4×n+1	Symmetrical
Second (Binary)	$\frac{V_{s1}}{2^0}=\frac{V_{s2}}{2^1}=\cdots=\frac{V_{sn}}{2^{n-1}}$	(4×2ⁿ)-3	Asymmetrical
Third (Ternary)	$\frac{V_{s1}}{3^0}=\frac{V_{s2}}{3^1}=\cdots=\frac{V_{sn}}{3^{n-1}}$	(2×3ⁿ)-1	Asymmetrical
Fourth	$V_{s1}=\frac{V_{s2}}{2}=\cdots=\frac{V_{sn}}{n}$	2×n(n+1)+1	Asymmetrical

IV. COMPARISON

Table V compares proposed topology with conventional topologies in terms of component count. Fig. 5 compares the number of IGBTs against the number of output voltage levels in the proposed symmetric and asymmetric topologies with other topologies. This figureshows that the proposed topology of multilevel inverter requires the least number of IGBTs and corresponding gate driver circuits than the other topologies [12-16].

TABLEV.COMPARISON OF PROPOSED SYMMETRIC TOPOLOGY WITH CONVENTIONAL TOPOLOGIES(THREEPHASE)

Components	NPC	Flying capacitor	CHB	Proposed topology
Main switches	6(N-1)	6(N-1)	6(N-1)	(3/2)(N+7)
Total diodes	3N(N-1)	6(N-1)	6(N-1)	3(N+3)
DC bus capacitors/ Isolated supplies	N-1	N-1	3(N-1)/2	(3/2)(N-1)
Flying capacitors	0	(3/2)(N-1)(N-2)	0	0
Total count	(N-1)(3N+7)	(1/2)(N-1)(3N+20)	(27/2)(N-1)	6(N+3)



(a) (b)

Fig. 5. Comparison of number of IGBTs against the number of voltage levels. (a) Symmetrical Configuration. (b) Asymmetrical Configuration.

V. SIMULATION AND EXPERIMENTALRESULTS

A. SimulationResults:

The proposed topology has been simulated using MATLAB/SIMULINK software for R-L load with R=100Ω, L=25mH. The frequency of the output voltage is takes as 50HZ. The parameters used for simulation and experimenthave been given in Table VI. The output voltage, current waveforms and its corresponding harmonic spectrum are shown in Fig. 7 and THD values are listed in the Table VII. Capacitor size of each unit is same for low voltage applications and different for high voltageapplications.

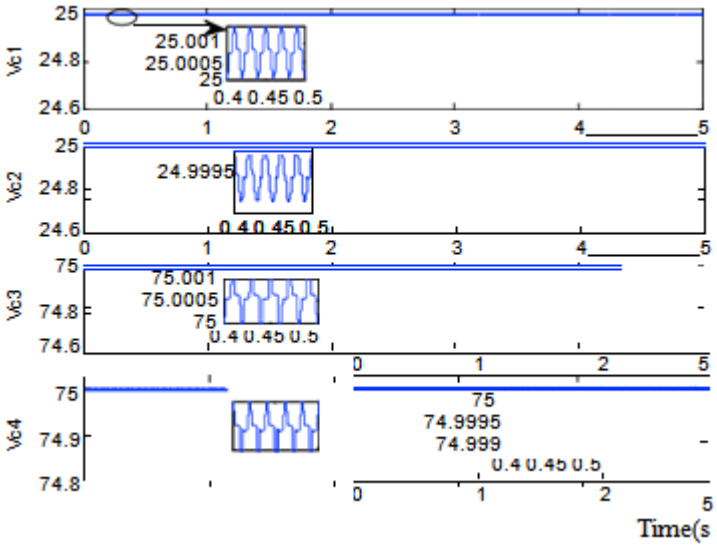


Fig. 6. Balanced capacitor voltage in 17-level topology

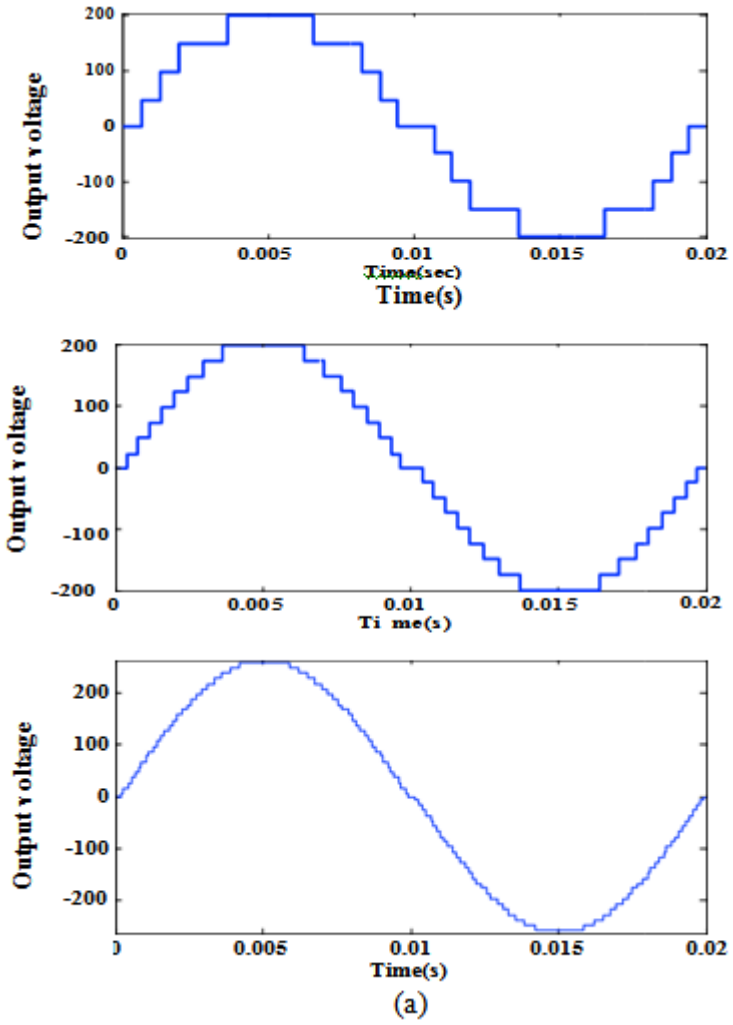


Fig. 7. Simulation results: (a) Output voltage. (b) THD corresponding to output voltage.

B. ExperimentalResults:

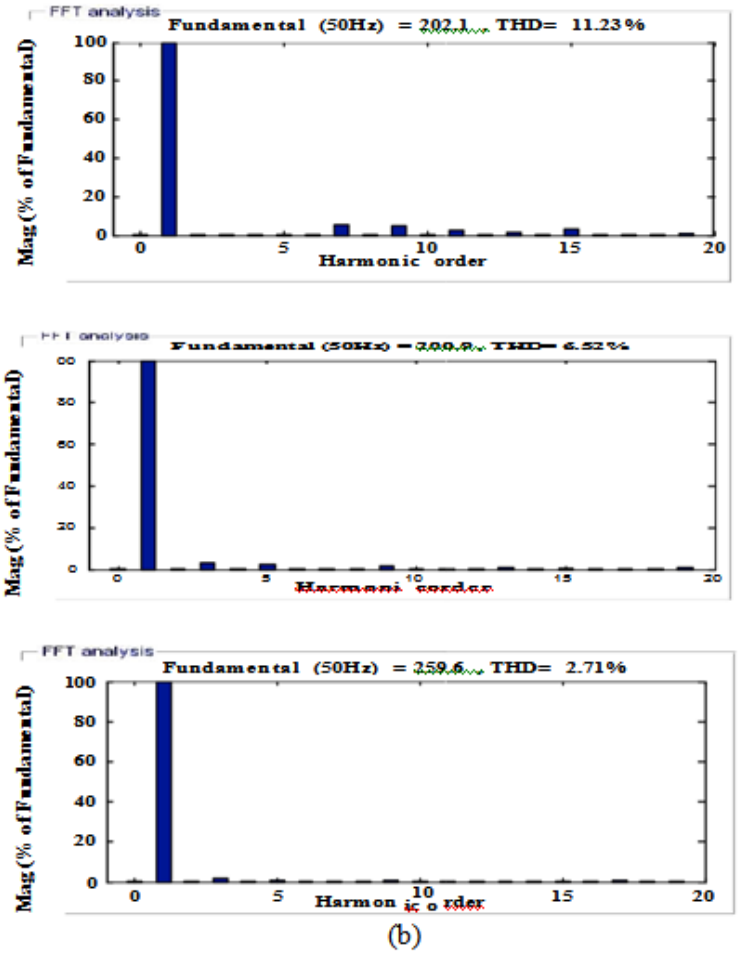
The experimental setup is shown in Fig. 8. Theswitching pattern has been implemented by us ngdSAPCE DS1104 controller. The experimental results for the proposed topology are shown in the Fig. 9.

TABLE VI. SIMULATION AND E PERIMENT PARAMETERS

Parameter	Simulation			Experimental	
	9-level	*17-level*	*53-level*	*9-level*	*17-level*
Vs1	100	50	20	10	10
Vs2	100	150	60	10	30
Vs3	-	-	180	-	-
Capacitor(μF)	1000	1000	1000	1000	1000
R(Ω)	100	100	100	50	50
L(mH)	25	25	25	10	10
Switching frequency(HZ)	100	100	100	100	100

TABLE VII. THD CORRESPONDING TO OUPUT VOLTAGE

S.NO	Output level	THD	
		Simulation	*Experimental*
1	9-level	11.23	11.90
2	17-level	6.52	6.90
3	53-level	2.71	-



(b)

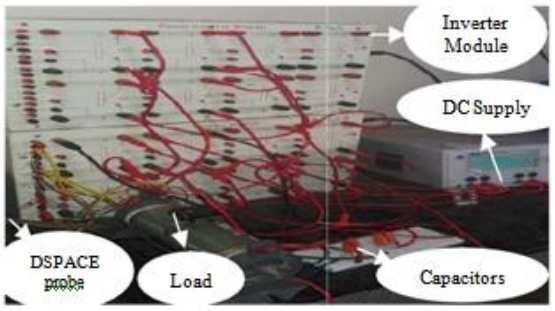
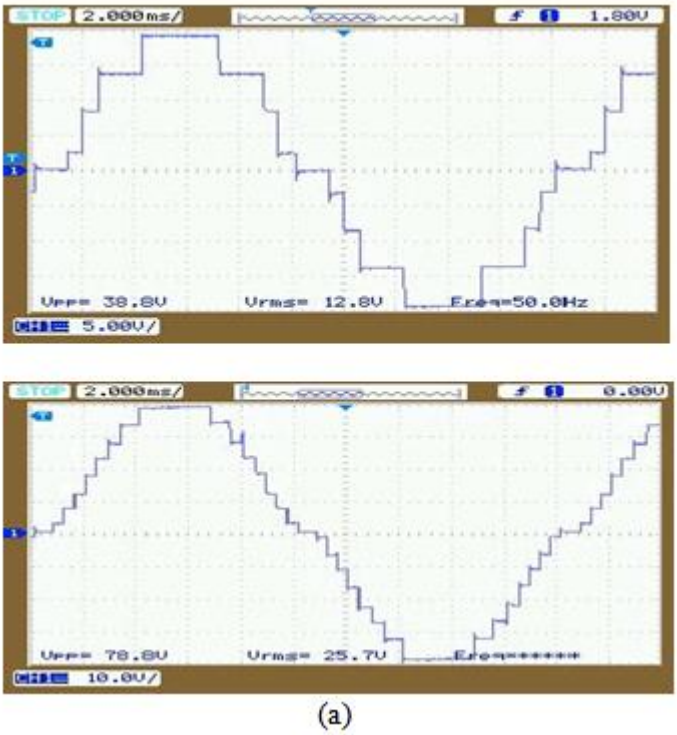


Fig. 8. Experimental setup



(a)

Fig. 9. Experimental results: (a) Output voltage (b) THD corresponding to output voltage

VI. CONCLUSION

In this paper new topology of MLI has been proposedThe proposed topology can produce highernumber ofoutput voltage levels for less number of controlled switches and isolated DC voltage sources. The switches in the level generator of proposed topology are having less blocking voltage capability thereby total blocking voltage capability of proposed MLI is less. Capacitor balancing has been achieved by properly selecting the switching states. The proposed algorithms help in generating higher number of voltage levels which lead to lower THD in output voltage.

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