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Development of Multicarrier SPWM Techniques for Cascaded MLI

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ABSTRACT
In this paper, investigates and analysis the performance of the novel pulse width modulation techniques which uses unipolar sine carrier waveform and staircase carrier waveform are proposed for five-level cascaded inverter. In each carrier waveform, different techniques such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The fundamental output voltage and harmonics obtained in each method are compared with the output waveform obtained with the triangular carrier waveform. The different PWM methodologies adopting the constant switching frequency multicarrier with different modulation indexes are simulated for a 1kW, 3φ cascaded multilevel inverter using MATLAB/SIMULINK and the effect of switching frequency on the fundamental output voltage and harmonics are also analyzed. The proposed switching technique enhances the fundamental component of the output voltage and reduces the total harmonic distortion.

Keywords: Modulation Index (MI), Staircase Multicarrier SPWM (SCMC SPWM), Total Harmonic Distortion (THD), Triangular Multicarrier SPWM (TMC SPWM), Unipolar Sine Multicarrier SPWM (USMC SPWM)

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I. Introduction

The multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveform [1]. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected [2].

In this paper, constant switching frequency multicarrier pulse width modulation method is used for the multilevel inverter [3]. The control objective is to compare the reference sine wave with multicarrier waves for three phase five level cascaded inverters. Multilevel voltage source inverter (MVSI) structure is very popular especially in high power DC to AC power conversion applications. It offers several advantages that make it preferable over the conventional voltage source inverter (VSI). These include the capability to handle higher DC link voltage; the stress on each switching device can be reduced in proportional to the higher voltages [4]. Consequently, in some applications, it is possible to avoid expensive and bulky step-up transformer. Another significant advantage of a multilevel output is better sinusoidal voltage waveform. As a result, a lower total harmonic distortion (THD) is obtained [5], [6]. The concept of multilevel converter has been introduced since 1975 [7]. The term multilevel began with the three-level converter [6]. Subsequently, several multilevel converter topologies have been developed, such as the Diode Clamped Multilevel Inverter (DCMLI) also known as Neutral Point Clamped (NPC) Inverter, Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded Multilevel Inverter (CCMLI) [8], [9]. Among them, CCMLI topology is the most attractive, since it requires the least number of components and increases the number of levels in the inverter without requiring high ratings on individual devices and the power rating of the CCMLI is also increased. It also results in simple circuit layout

and is modular in structure. Furthermore, CCMLI type of topology is free of DC voltage balancing problem, which is a common issue facing in the DCMLI and FCMLI topologies [10], [11].
Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly [12]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for high power application [13]
In motor applications, high dv/dt in power supply generates high stress on motor windings and requires additional motor insulation. Further; high dv/dt of semiconductor devices increases the electromagnetic interference (EMI), common-mode voltage and possibilities of failure on motor [14], [15]. By increasing the number of levels in the output waveform, the switching dv/dt stress is reduced in the multilevel inverter [16], [17]. Multilevel inverters are suitable for power electronics applications such as flexible ac transmission systems, renewable energy sources, uninterruptible power supplies, electrical drives and active power filters.

II. Cascaded Multilevel Inverter

The single-phase structure of three phase five-level cascaded inverter is illustrated in Figure 1. Each separate dc source is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter can generate three different outputs voltage level, $+V_{dc}$, 0 and $-V_{dc}$, by connecting the dc source to the ac output by different switching combinations of the four semiconductor switches S1, S2, S3 and S4. To obtain $+V_{dc}$, switches S1 and S2 are tuned on, whereas $-V_{dc}$ can be obtained by tuning on switches S3 and S4, By turning on S1 and S3 or S2 and S4, the output voltage is 0, The ac outputs of each of the full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [18], [19].
The CCMLI is producing five level output and they are $2V_{dc}$, V_{dc}, 0, $-V_{dc}$ and $-2V_{dc}$. This topology is suitable for applications where separate dc voltage sources are available, such as photovoltaic (PV) generators, fuel cells and batteries. The phase output voltage is generated by the sum of two output voltage of the full bridge inverter modules. The circuit in Figure1 utilizes two independent dc sources and consequently will create an output phase voltage with five-level. In general, if N is the number of independent dc sources per phase, then the following relations apply [20]:

$$m = 2N + 1 \quad (1)$$

$$q = 2(m-1) \quad (2)$$

Where m is the number of levels and q is the number of switching devices in each phase
The most well known SPWM which can be applied to a CCMLI is the Phase-Shifted SPWM. This modulation technique is the same as that of the conventional SPWM technique which is applied to a conventional single phase full-bridge inverter, the only difference being that it utilizes more than one carrier. The number of carriers to be used per phase is equal to twice the number of dc voltage sources per phase (2N) [21]. Figure 2 presents the simulation model of a three-phase five-level CCMLI and is developed using MATLAB/SIMULINK. The simulation results are obtained for the output phase voltage and line voltage of the three phase five-level CCMLI with 1kW, 3φ resistive loads for various PWM techniques.

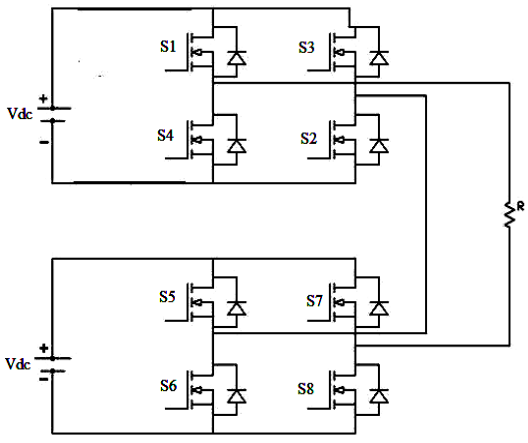


Figure 1 1φ structure of five-level CCMLI

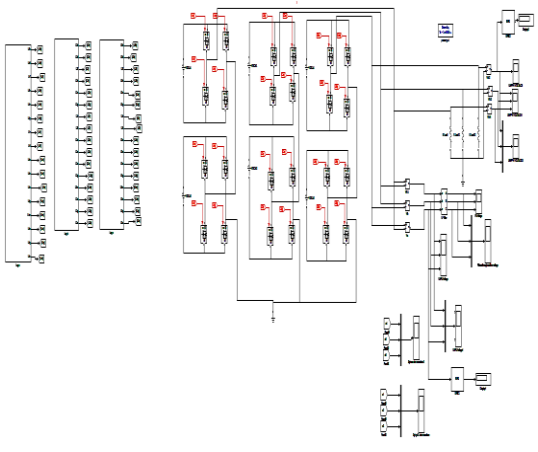


Figure 2 Simulation model of 3φ five-level CCMLI

III. Modulation Techniques

The Pulse Width Modulation (PWM) control strategies development tries to reduce the total harmonic distortion (THD) of the output voltage. Any deviation in the output voltage of the sinusoidal wave shape will result in harmonic currents in the load and this harmonic current produces the electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonic and associated sideband harmonics away from the fundamental frequency component [22]. This increased switching frequency reduces harmonics, which results in a lower THD with high quality output voltage waveforms of desired fundamental RMS value and frequency which are as close as possible to sinusoidal wave shape [23].

The carrier frequency defines the switching frequency of the converter and the high order harmonic components of the output voltage spectrum and the sidebands occur around the carrier frequency and its multiples. The higher switching frequency can be employed for low and medium power inverters, whereas, for high power and medium voltage applications the switching frequency should be low. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy [24], [25]. The three phase multi level inverter requires three modulating signals or reference signals which are three sine-waves with 120 degree phase shift and equal in magnitudes. In this paper, new carrier based PWM techniques are developed which are as, Unipolar Sine Multicarrier Sinusoidal PWM (USMC SPWM) and Staircase Multicarrier Sinusoidal PWM (SCMC SPWM). Each carrier is to be compared with the corresponding modulating sine wave [26], [27]. The reference or modulation waveform has peak amplitude A_r and frequency f_r and it is centered in the middle of the carrier set. The general principle of a carrier based PWM technique is the comparison of a sinusoidal waveform with a carrier waveform, this typically being a triangular carrier waveform. The reference is continuously compared with the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched off [28], [29]. In multilevel inverters, the amplitude modulation index, M_a and the frequency ratio, M_f are defined as,

$$M_a = \frac{A_r}{(m-1)A_c} \tag{3}$$

$$M_f = \frac{f_c}{f_r} \tag{4}$$

Where A_r and A_c are amplitude of reference and carrier signal respectively. f_r and f_c are frequency of reference and carrier signal respectively.

In this paper, modulation indexes used are 0.6, 0.7, 0.8, 0.9 and 1 for five-level CCMLI. For multilevel applications, carrier based PWM techniques with multiple carriers are used. The Multicarrier Modulation (MCM) techniques, can be divided in to the following categories such as [30], [31],

1. Phase disposition (PD) where all the carriers are in phase.
2. Inverted phase disposition (IPD) where all the carriers are in phase and is inverted.
3. Phase opposition disposition (POD) where the carriers above the zero reference are in phase but shifted by 180 degrees from those carriers below the zero reference.
4. Alternative phase opposition disposition (APOD) where each carrier band is shifted by 180 degrees from the adjacent carrier bands [2].

The above modulation strategies are implemented for different carriers such as unipolar sine wave and staircase wave. The phase voltage and line voltage waveform, harmonic spectrums of the line voltage are shown for different modulation techniques by doing simulation using MATLAB/SIMULINK for five-level CCMLI and the results obtained are compared.

3.1. Triangular Multicarrier Sinusoidal PWM (TMC SPWM)

The performance of the multilevel inverter is based on the multi carrier modulation technique used. Two-level to multilevel inverters are made using several triangular carrier signals and one reference signal per phase. Carrara [5] developed multilevel sub harmonic PWM (SH-PWM), which is as follows, for m-level inverter, m-1 carriers [32] with the same frequency f_c and same amplitude A_c are disposed such that the bands they occupy are contiguous. They are defined as

$$C_i = A_c\left((-1)^{f(i)} y_c(\omega_c, \varphi) + t - \frac{m}{2}\right), \quad i = 1, \ldots\ldots (m-1) \tag{5}$$

Where y_c is a normalized symmetrical triangular carrier defined as,

$$y_c(\omega_c, \varphi) = (-1)^{[\alpha]}((\alpha \bmod 2) - 1) + \frac{1}{2} \tag{6}$$

$$\alpha = \frac{\omega_c t + \varphi}{\pi}, \omega_c = 2\pi f_c \tag{7}$$

φ represents the phase angle of y_c. y_c is a periodic function with the period $T_C = \frac{2\pi}{\omega_C}$. It is shown that using symmetrical triangular carrier generates less harmonic distortion at the inverters output [33], [34]. The carrier waveforms, output voltage waveforms and %THD chart are shown only for selected PWM techniques in order to restrict the number of figures.

In TMC SPWM, so far only the PD, POD and APOD techniques are discussed earlier in the literature. In this paper, IPD scheme is also applied to TMC SPWM and it is found that this scheme gives the lowest THD among the TMC SPWM schemes. The multicarrier modulation techniques (PD, IPD, POD and APOD) are implemented using triangular multicarrier signals for five-level CCMLI with different modulation indexes and are shown in Figure 3(a) and 3(b) respectively.

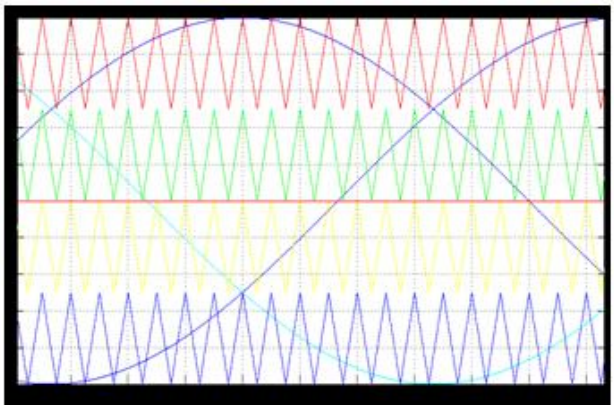


Figure 3(a): IPD TMC SPWM with Ma=1

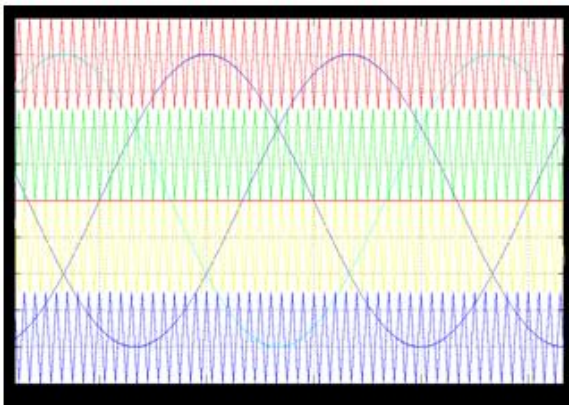


Figure 3(b): POD TMC SPWM with Ma=0.8

3.2. Unipolar Sine Multicarrier Sinusoidal PWM (USMC SPWM)

In this PWM technique, the sinusoidal signal is converted in to the unipolar sinusoidal signal [35]. The entire negative half cycles in the waveform is converted into positive half cycles with the same amplitude and frequency. This signal is same as that of the full wave rectifier output. That is the signal has only continuous positive half cycles. This is called unipolar sine wave. The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses a high frequency sine carrier that helps to maximize the output voltage for a given modulation index [36]-[38]. The multicarrier modulation techniques (PD, IPD, POD and APOD) are implemented using unipolar sine multicarrier signals for five level CCMLI with different modulation indexes and are shown in Figure 4(a) and 4(b) respectively.

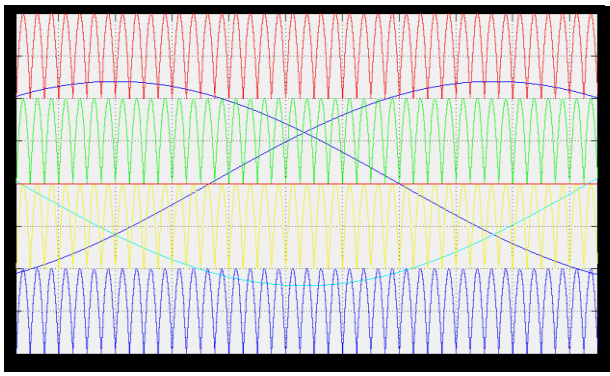


Figure 4(a): PD USMC SPWM with Ma=0.6

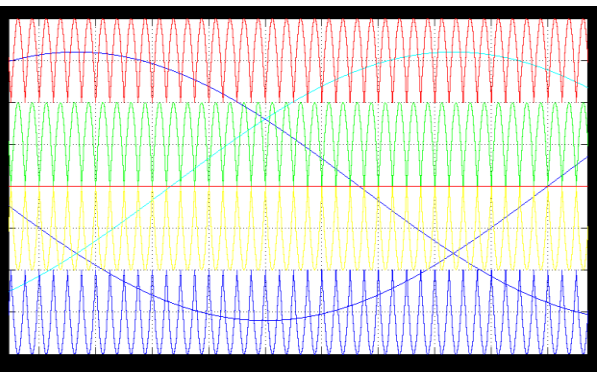


Figure 4(b): POD USMC SPWM with Ma=0.8

3.3. Staircase Multicarrier Sinusoidal PWM (SCMC SPWM)

Staircase wave is also known as approximated or modified triangular wave and is obtained from the repeated sequence carrier wave by limiting its magnitude to $A_{c;}$ it is obtained from simulink block, Stair case wave is the periodic signal which passes its input signal through a stair-step function so that many neighboring points on the input time axis are mapped to one point on the output magnitude axis. The effect is to make a smooth stair-step signal. The output is computed using the round-to-nearest method, which produces an output that is symmetric about zero.

$$y_q = q \times \left(\frac{u}{n}\right), (0 \le t \le \frac{T}{2}) \qquad (8)$$

$$y = 2\left(1 - \frac{t}{T}\right), \left(\frac{T}{2} \le t \le T\right) \quad (9)$$

Where q is the step number = 1, 2... 8, n is the max number of steps = 8, y is the output, u is the peak voltage and T is the period of staircase waveform. After the maximum step (magnitude), the magnitude reduces linearly and comes to zero and the process repeats. The number of steps for each stair case wave is nine.
The multicarrier modulation techniques (PD, IPD, POD and APOD) are implemented using staircase multicarrier signals for five level CCMLI with different modulation indexes and are shown in Figure 5(a) and 5(b) respectively.

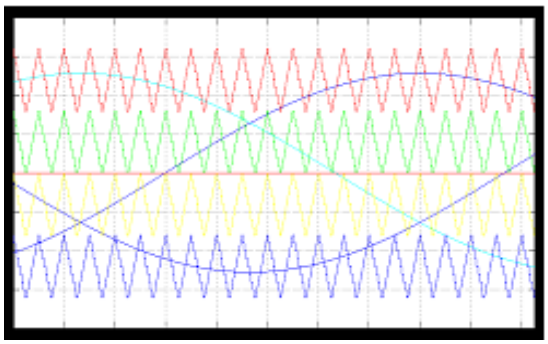


Figure 5(a): IPD SCMC SPWM with Ma=0.8

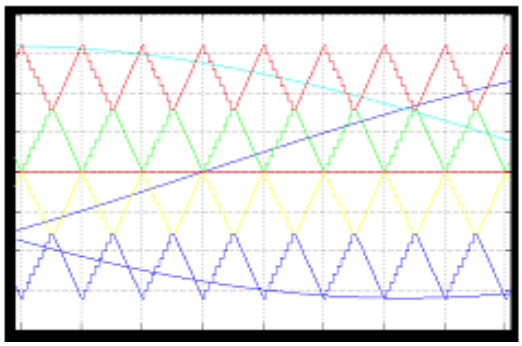


Figure 5(b): APOD SCMC SPWM with Ma=1

IV. Simulation Results

The five level cascaded multilevel inverter model with different modulation indexes was implemented in MATLAB/SIMULINK software to demonstrate the feasibility of PWM techniques. Phase disposition, inverted phase disposition, phase opposition disposition and alternative phase opposition disposition techniques are used for the various multicarrier SPWM techniques such as

1. Triangular Multicarrier Sinusoidal PWM
2. Unipolar Sine Multicarrier Sinusoidal PWM
3. Staircase Multicarrier Sinusoidal PWM

The line voltage waveform with its harmonic spectrum at fundamental frequency of 50Hz and switching frequency of 2kHz and 10kHz are obtained for the proposed CCMLI. For comparison, the total harmonic distortion (THD) was chosen to be evaluated for all the modulation techniques. In order to get THD level of the waveform, a Fast Fourier Transform (FFT) is applied to obtain the spectrum of the output voltage. The THD is calculated using the following equation in this work.

$$THD = \frac{\sqrt{\sum_{n=2}^{80} v_n^2}}{v_1} \quad (10)$$

Where n is the harmonic order, v_n is the RMS value of the n^{th} harmonic component and v_1 is the RMS value of the fundamental component. Here the %THD is calculated up to a harmonic order which is twice the switching frequency. For 2kHz switching frequency up to 80^{th} order harmonics is taken in to account for calculating THD and for 10kHz switching frequency up to 400^{th} order harmonics is taken in to account for calculating THD.

4.1. Triangular Multi Carrier SPWM (TMC SPWM)

Figure 6(a) and 6(b) show the line voltage waveforms and the percentage THD of the line voltage for five level using the inverted phase disposition technique for triangular multi carrier sinusoidal PWM with Ma=1.

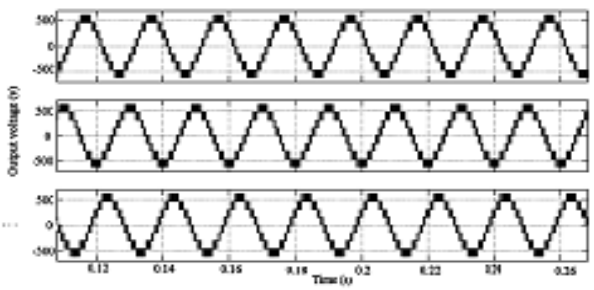


Figure 6(a): Line Voltage for IPD SPWM with Ma=1

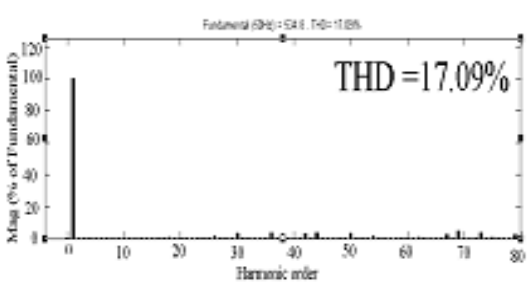


Figure 6(b): Line Voltage %THD for IPD SPWM with Ma=1

Table 1 shows the percentage line voltage THD for the five-level CCML with triangular multicarrier signal with different multicarrier PWM techniques with a switching frequency of 2kHz and 10kHz respectively for different modulation indexes.

Table1: Line voltage %THD for TMC SPWM

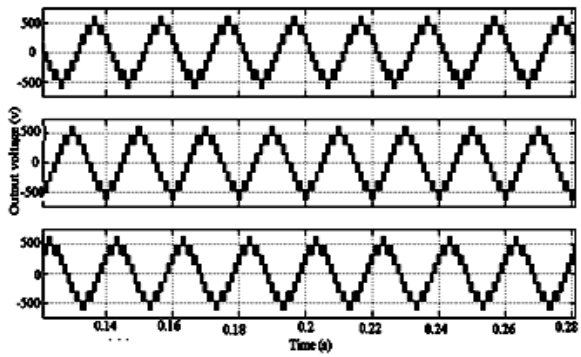
Modulation Technique	Line voltage %THD									
	2kHz					10kHz				
	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6
PD	17.11	17.55	21.73	24.14	25.62	17.58	17.77	21.81	24.21	28.03
IPD	**17.09**	17.55	21.73	24.14	25.62	**17.56**	17.77	21.81	24.21	28.03
POD	21.89	29.94	35.48	38.65	38.42	23.91	31.42	36.45	38.63	37.68
APOD	25.66	28.75	29.75	28.04	25.93	27.07	29.57	30.46	28.85	29.33

From the above table, it is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is increased for the PD and IPD schemes with all modulation indexes. In the POD scheme, if the switching frequency is increased, the percentage line voltage THD is reduced with modulation index of 0.7 and 0.6. In the APOD scheme, when the switching frequency is increased, the percentage line voltage THD is increased with all modulation indexes, in five-level CCMLI. From the simulation result in the triangular multicarrier SPWM technique PD and IPD PWM schemes, from 3rd order harmonics to 25th order harmonics are less than 1%. Few of the odd and even order harmonics from 26th harmonics to 79th harmonics are present. The dominant 69th harmonic factor is about 5% for the PD and IPD schemes. In the POD scheme, from 3rd odd order harmonics to 27th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 29th harmonics to 79th harmonics are 1% to 3%. The dominant 39th and 41st harmonic factor are 10.29% and 10.46% respectively for the POD scheme. In the APOD scheme, from 3rd odd order harmonics to 31st odd order harmonics are less than 1% and all even order harmonics are 0.03%. Few of the odd order harmonics from 33rd harmonics to 79th harmonics are present. The dominant 35th and 45th harmonic factor are 11.94% and 11.87% respectively for the APOD scheme.

It is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is increased very slightly and the fundamental phase and line voltage are decreased for the PD and IPD schemes. In the POD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD is increased and the fundamental phase and line voltage are decreased very slightly. Also the fundamental line voltage is maximum for APOD scheme and is minimum for PD and IPD schemes.

4.2. Unipolar Sine Multi Carrier SPWM (USMC SPWM)

Figure 7(a) and 7(b) show the line voltage waveforms and the percentage THD of the line voltage for five-level using the inverted phase disposition technique for unipolar sine multicarrier sinusoidal PWM with Ma=0.9.



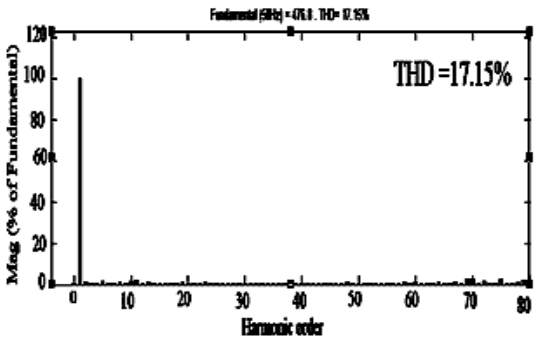


Figure 7(a): Line Voltage for IPD SPWM with Ma=0.9 Figure 7(b): Line Voltage %THD for IPD SPWM with Ma=0.9

Table 2 shows the percentage line voltage THD for the five and three level CCML with unipolar sine multicarrier signal with different multicarrier PWM techniques with a switching frequency of 2kHz and 10kHz respectively for different modulation indexes.

Table 2: Line voltage %THD for USMC SPWM

Modulation Technique	Line voltage %THD									
	2kHz					10kHz				
	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6
PD	17.67	**17.15**	20.49	23.38	26.24	18.09	**16.89**	19.82	23.21	27.24
IPD	17.67	**17.15**	20.49	23.38	26.24	18.09	**16.89**	19.82	23.21	27.24
POD	27.89	36.16	39.83	41.02	41.68	28.39	35.17	41.86	43.56	49.48
APOD	26.70	28.81	30.14	29.80	27.44	30.48	29.00	27.90	34.10	29.38

From the above table, it is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is increased for the PD and IPD schemes with modulation index of 1and 0.6. In the POD scheme, if the switching frequency of the CCMLI is increased, the percentage line voltage THD is reduced with modulation index of 0.9. In the APOD scheme, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is reduced with modulation index of 0.8, in five-level CCMLI. If the output voltage level increases the percentage line voltage THD decreases. From the simulation result in the unipolar sine multi carrier SPWM technique PD and IPD PWM schemes, from 3rd order harmonics to 66th order harmonics are less than 1%. Few of the higher odd order harmonics and even order harmonics from 67th harmonics to 79th harmonics for the above mentioned scheme are less than 3%. The dominant 76th harmonic factor is about 3% for the PD and IPD schemes. In the POD scheme, from 3rd odd order harmonics to 5th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 7th harmonics to 79th harmonics are 1% to 2%. The dominant 73rd and 79th harmonic factor are 6.82% and 15.00% respectively for the POD scheme. In the APOD scheme, from 3rd odd order harmonics to 5th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 7th harmonics to 79th harmonics are present. The dominant 73rd and 75th harmonic factor are 6.56% and 10.50% respectively for the APOD scheme.

It is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is increased very slightly and the fundamental phase and line voltage are decreased for the PD and IPD schemes. In the POD scheme, if the switching frequency is increased, the percentage line voltage THD, the fundamental phase and line voltage are increased. In the APOD scheme, when the switching frequency is increased, the percentage line voltage THD is increased and the fundamental phase and line voltage are decreased. Also the fundamental line voltage is maximum for APOD scheme and is minimum for PD and IPD scheme.

4.3. Staircase Multi Carrier SPWM (SCMC SPWM)

Figure 8(a) and 8(b) show the line voltage waveforms and the percentage THD of the line voltage for five-level using the phase disposition technique for staircase multicarrier sinusoidal PWM with Ma=0.9.

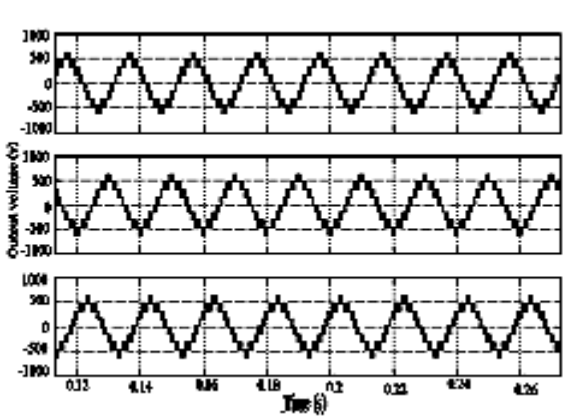


Figure 8(a): Line Voltage for PD SPWM with Ma=0.9

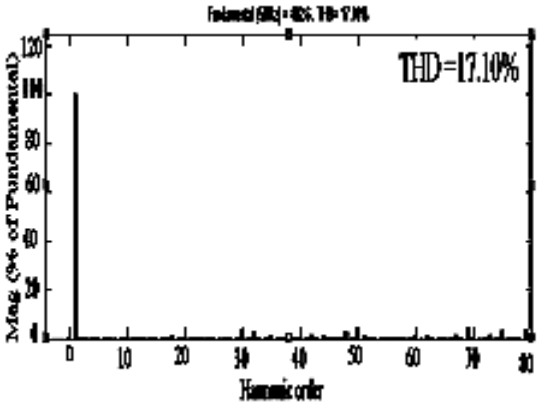


Figure 8(b): Line Voltage %THD for PD SPWM with Ma=0.9

Table 3 shows the percentage line voltage THD for the five-level CCML with staircase multicarrier signal for different multicarrier PWM techniques with a switching frequency of 2kHz and 10kHz respectively for different modulation indexes.

Table 3: Line voltage %THD for SCMC SPWM

Modulation Technique	**Line voltage %THD**									
	2kHz					**10kHz**				
	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6	M_a=1	M_a=0.9	M_a=0.8	M_a=0.7	M_a=0.6
PD	17.22	**17.10**	21.38	24.04	25.38	17.18	**17.15**	21.75	24.18	26.54
IPD	17.20	**17.10**	21.38	24.04	25.38	17.16	**17.15**	21.75	24.18	26.54
POD	21.71	29.42	35.56	38.88	39.14	23.24	29.28	35.74	39.24	39.56
APOD	25.90	28.78	30.17	28.53	26.55	26.74	28.41	30.18	28.82	27.13

From the above table, it is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is reduced for the PD and IPD schemes with modulation index of 1. In the POD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD is reduced with modulation index of 0.9 in five level CCMLI. If the output voltage level increases the percentage line voltage

THD decreases. From the simulation result in the proposed staircase multi carrier SPWM technique PD and IPD PWM schemes, from 3rd order harmonics to 25th order harmonics are less than 1% and are negligible. Few of the odd and even order harmonics from 26th harmonics to 79th harmonics are 1% to 3%. The dominant 69th harmonic factor is about 5% for the PD and IPD schemes. In the POD PWM scheme, from 3rd odd order harmonics to 27th odd order harmonics are less than 1% and all even order harmonics are 0.03%. Few of the odd order harmonics from 29th harmonics to 79th harmonics are present. The dominant 39th and 41st harmonic factor are 10.05% and 9.97% respectively for the POD scheme. In the APOD PWM scheme, from 3rd odd order harmonics to 31st odd order harmonics are less than 1% and all even order harmonics are 0.03%. Few of the odd order harmonics above 33rd harmonics are present. The dominant 35th and 45th harmonic factor are 11.61% and 11.43% respectively for the APOD scheme.

It is observed that when the switching frequency of the CCMLI is increased, the percentage line voltage THD, the fundamental voltage for phase and line are decreased very slightly for the PD and IPD schemes. In the POD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD is increased very slightly and the fundamental voltage for phase and line voltage are decreased very slightly. Also the fundamental line voltage is maximum for POD and APOD schemes and is minimum for PD and IPD schemes.

V. Conclusion

In this paper, the performance of different multicarrier PWM techniques which uses triangular multicarrier waveform, unipolar sine multicarrier waveform and staircase waveform in multilevel inverters are found out. In all the above PWM techniques, different modulation strategies such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The results are verified by doing simulation for a 1kW, 3φ five-level cascaded inverter in MATLAB/SIMULINK. The output quantities like fundamental phase and line voltage, percentage THD of the line voltage and percentage dominant harmonic factor are measured in the all the above PWM schemes and the results are compared.

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