ISSN (e): 2250 – 3005 || Volume, 06 || Issue, 03||March – 2016 ||
International Journal of Computational Engineering Research (IJCER)

Double feedback technique for reduction of Noise LNA with gain enhancement

[1]K. RAJU M.Tech, [2]R.SIREESHA M.Tech, [3]K.VIJAY KUMAR M.Tech
[1](Assistant Professor, Dept. of ECE, G.Pulla Reddy Engineering College, Kurnool)
[2](Assistant Professor, Dept. of ECE, Brindavan Institute of Technology and Science, Kurnool)
[3](Assistant Professor, Dept. of ECE, Ravindra College Of Engineering For Women, Kurnool)

Abstract
In this paper we present a balun low noise amplifier (LNA) in which the gain is boosted by using a double feedback structure. The circuit is based on a conventional balun LNA with noise and distortion cancelation. The LNA is based on the combination of a common-gate (CG) stage and common-source (CS) stage. We propose to replace the load resistors by active loads, which can be used to implement local feedback loops (in the CG and CS stages). This will boost the gain and reduce the noise figure (NF). Simulation results, with a 130nm CMOS technology, show that the gain is 24dB and the NF is less than 2.7dB. The total power dissipation is only 5.4mW (since no extra blocks are required), leading to a figure-of-merit (FOM) of 3.8mW^{-1} using a nominal 1.2V supply. Measurement results are presented for the proposed DFBLNA included in a receiver front-end for biomedical applications (ISM and WMTS).

Keywords : *RF front-end receivers CMOS LNAs Noise reduction Wideband LNA*

I. Introduction

Wireless communications for Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications are found to be low cost, require low power, low voltage Transceivers, fully integrated on a single chip. The LNA is a Key block in these systems and will be investigated in this paper. Wideband LNAs with high gain and low noise figure (NF), using noise and distortion cancelation have been proposed, but these circuits have large power dissipation for high gain and low noise figure.

In this paper our main goal is to design a very low area and low cost LNA, with very high gain and low NF using 1.2V supply. This is obtained by replacing the load resistors by transistors biased close to saturation .In a circuit operating at 1.2V with controllable gain was proposed .In an LNA with double feed forward (DFF) has been used. In this paper we investigate the possibility of using a double feedback (DFB) technique to boost the gain and reduce the noise figure (NF).

Equations for gain and noise figure are presented, which can be used to optimize the circuit performance .A circuit proto type in a 130nm standard CMOS technology at1.2V has been designed and simulated to demonstrate the proposed technique. Simulation results show a gain of 24dB and NF below 2.7dB, with power
Dissipation of only 5.4mW, leading to a FOM of 3.8mW-1, which is, to the authors 'knowledge, the best FOM in the literature for LNAs with nominal 1.2V supply.

Measurement results for the proposed DFBLNA where it is included in a modern receiver are also presented, which prove that the proposed approach leads to a high gain, low NF circuit, when compared with other state-of-the-art approaches.

II. Balun LNA with noise reduction

In a receiver, the antenna and RF filters are typically single-ended, so it is very desirable to have an LNA with single-ended input. A differential signal in the receiver is preferred to reduce harmonic distortion and to reject power supply and substrate noise. Traditionally, an external balun is used to convert single-ended signals to differential, but it introduces losses and degrades the receiver NF. A balun LNA converts a single-ended to a differential signal, which simplifies the receiver design, by avoiding the external balun.

The circuit proposed in and shown in Fig. 1 is a balun LNA, in which the thermal noise of M_1 (main source of noise) is cancelled out. The noise produced by M_1 appears in phase at the two output terminals, while the signals at these terminals are in opposition. Thus, at the differential output the gain is doubled and the noise is cancelled. It can be shown that the distortion introduced by M_1 is also cancelled.

The differential voltage gain of the LNA is obtained from the difference of the common-gate (CG) and the common-source (CS) stage gains:

$$A_{V,Diff} = g_{m1}(R_1 \backslash\backslash r_{ds1}) + g_{m2}(R_2 \backslash\backslash r_{ds2}) \quad (1)$$

where r_{ds} is the transistors output resistance and g_m is the transconductance. The input impedance is given, approximately, by

$$Z_{in} = \frac{1}{g_{m1}} \quad (2)$$

III. Proposed circuit

The circuit in Fig. 1 cannot operate at low supply voltage with high gain, due to the large voltage drop at the resistors. Based on the CG–CS LNA circuit of Fig.1, we investigate a circuit using active loads, in which the load resistors are replaced by transistors biased in the triode region, which behave, approximately, as linear resistors.

In a method was proposed to obtain gain boosting in the LNA of Fig. 1, which was referred to as double feed-forward (DFF) LNA, since it consisted of the use of two feed-forward loops, as shown in Fig. 2.

Since the CG stage gain is limited by the input matching, an Inverter based block with gain α is applied (this inversion is required, since the CG stage does not change the input signal phase) in the feed forward path. This modification provides gain boosting and an additional degree of free domain the design. At the same time the input signal is also applied at CS stage through a feed forward loop, but in this case there is no need of an inverter, and the CS gain can be adjusted through Vb2. Despite the significant gain boosting this circuit provides, its linearity and bandwidth are degraded. Here we propose an alternative method of gain boosting, which uses two local feedback loops as shown in Fig.3. This circuit will be referred to here as double feedback (DFB) LNA. A DFB LNA is a simpler circuit than DFF LNA (hence, with Lower area and power), and produces a higher gain increase and more NF reduction.

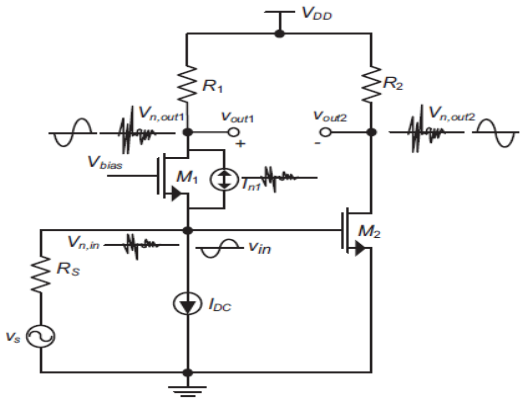

Fig.1. Balun LNA with cancelling of the noise of the CG-transistor M1

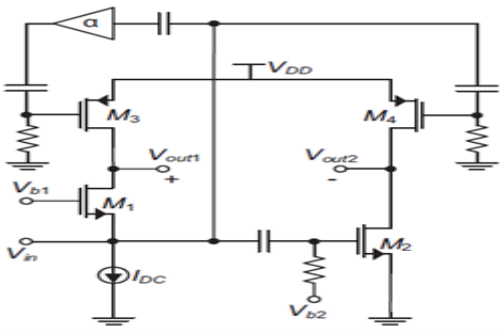

Fig.2. LNA using double feedforward (DFF)

In the DFB LNA (Fig.3), V_{in} after amplification in the CG stage (M_1) is applied to the gate of M_4, being further amplified and added to V_{out2}. The resulting signal is amplified trough M_3, and added to V_{out1}. With this structure there is a significant gain increase, without using extra circuitry.

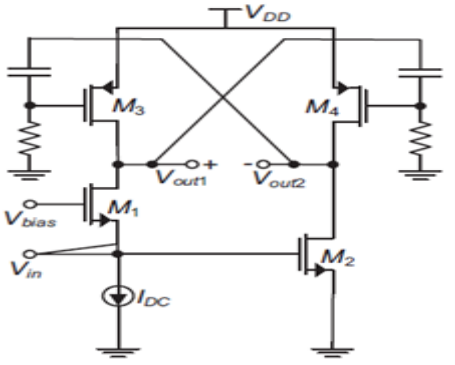

Fig.3. Proposed LNA using double feedback (DFB).

In the proposed circuit the main drawback is the reduction of the bandwidth due to the parasitic capacitances of M_3 and M_4, but the main goal is achieved: high gain and low NF.

The PMOS loads could be biased under saturation, which would lead to a higher gain due to the increase of the channel resistance. However, the circuit would be sensitive to DC variations, requiring a common-mode feedback (CMFB) type regulation circuit to compensate these variations, and consequently, adding more complexity to the circuit. Moreover, in the presence of miss-matches, noise cancelation is still partially cancelled, but distortion cancelation will be severely degraded.

The gain of the CG and CS stages is

$$\frac{V_{out1}}{V_{in}} = \frac{g_{mCG}g_2 + g_{m2}g_{m3}}{g_1g_2 - g_{m3}g_{m4}} \quad (3)$$

$$\frac{V_{out2}}{V_{in}} = \frac{g_{m2}g_{m1} + g_{mCG}g_4}{g_1g_2 - g_{m3}g_{m4}} \quad (4)$$

$$g_1 = g_{ds1} + g_{ds3} \text{ and } g_2 = g_{ds2} + g_{ds4}$$

Using (3) and (4), we obtain the LNA differential gain:

$$A_{v,Diff} = \frac{V_{out1} - V_{out2}}{V_{in}}$$

$$= \frac{gmCG(g_{m4} + g_2) + g_{m2}(g_{m3} + g_1)}{g_1g_2 - g_{m3}g_{m4}} \quad (5)$$

The input impedance is $Z_{in} = \frac{g_1g_2 - g_{m3}g_{m4})}{g_{mCG}(g_2g_{ds3} - g_{m3}g_{m4}) - g_{m2}g_{m3}g_{ds1}}$ (6)

Using Eqs. (5) and (6), we can optimize the circuit performance in order to increase the gain, while minimizing the impact on the input matching.

If it is assumed that $g_{m1} = g_{m2} = g_m$, the noise factor is

$$F_{LNA} = 1 + \frac{\gamma}{2R_Sg_m} + \frac{k_f}{8kTR_SC_{OX}f^{a_f}}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2} + \frac{1}{W_3L_3} + \frac{1}{W_4L_4}\right) \quad (7)$$

where k is Boltzmann's constant, c_{ox} is the oxide gate capacitance per unit area, W_1 and L_1 are the transistor dimensions, T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors. The main noise sources in this type of LNAs are those of M_1 (the thermal noise is cancelled) and those of M_2, while the noise introduced by the loads can be neglected.

From [6], to improve the noise figure, g_{m2} should be higher than g_{m1}, while g_{ds4} is increased to keep the output signals balanced:

$g_{m2} = \alpha . g_{m1}$

$g_{ds4} = \alpha . g_{ds3}$

The optimal value of α is obtained by simulation and it was found to be approximately 1.5.

IV. Simulation results

4.1. Comparison of DFB LNA with related circuits

The proposed circuit was designed using Cadence Spectre RF Simulator (SP, PSS, and PNOISE), using BSIM v3.3 models from standard CMOS 130nm technology with 1.2V supply. The circuit parameters are given in Table1. The transistors have minimum length to maximize speed, and V_{bias} is 795mV.

In Table 2 we compare the theoretical and simulation results for the optimized voltage gain. We use Eq. (1) for the LNA of Fig. 1 with resistors and for the circuit using active loads with MOS transistors biased in triode , Eq. (3) from is used for DFF LNA, and Eq. (5) for the proposed DFB circuit.

In order to investigate the influence of DFB on the LNA key parameters: gain, noise figure, linearity, and frequency band, several simulation results are presented in Table3. The circuits were designed for gain optimization and under the same conditions, with ideal biasing circuitry and with an ideal current source biased with 2mA, to highlight the advantages and trade-off of each circuit. For a convenient comparison of the results obtained, the following figure of merit is used

$$FOM_1\left[mW^{-1}\right] = \frac{Gain}{(F-1)P_{DC}\left[mW\right]} \quad (8)$$

The results in Table3 show that the DFB leads to the highest gain and the lowest NF, leading to the highest FOM. The dis-advantages are the increase of the circuit non-linearity and the reduction of the bandwidth.

Table1 : LNA circuit parameters using DFB.

Transistor	I_D (mA)	W (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
M_1	2	139.2	420	2.38	30.7
M_2	2.4	358.4	355	2.82	44.4
M_3	2	13.1	236	4.24	2.1
M_4	2.4	16.2	187	5.35	2.5

4.2. Proposed DFB prototype

In order to have a complete LNA prototype, we have included the biasing circuitry in simulations, which has lead to some degradation in the noise figure, mainly due to the current source. In Figs. 4–6, the simulation results for the input matching (S11), gain, and NF, for the proposed DFB circuit prototype are presented.

Comparing these results with state-of-the-art inductor less LNAs (Table4), we observe that our circuit is very good in terms of gain and NF, and has very low power, which leads to the best FOM1 (it should be noted that while some of the results in the references in Table4 are from measurements, our results are obtained by simulation, and some degradation is to be expected in the fabricated circuit). However, in order to have a fair comparison, we also present the extrapolated results for the DFB LNA from the measured data of the RF front-end and we have attributed all the losses to the LNA to assure that the real results are in fact better than the extrapolated ones. Since the LNAs have many performance parameters we have also included a second FOM (9) in Table4 that includes IIP3 and bandwidth.

$$FOM_2[-] = \frac{Gain.IIP3\left[mW\right].f_c\left[GHz\right]}{(F-1).P_{DC}\left[mW\right]} \quad (9)$$

This FOM was originally used for narrow band LNAs since the frequency of operation is considered instead of the bandwidth, which we have replaced here for a proper comparison of wideband LNAs.

The proposed circuit approach is especially interesting in low power and low voltage biomedical applications, since in these applications low power is a key requirement and some non-linearity can be tolerated. There are ISM bands at 450MHz and 900MHz and a WMTS band at 600MHz, for which the circuit proposed here can be a good alternative to the conventional solutions

Table2 : Optimized voltage gain(dB) for different topologies.

Load	Resistor [6]	MOS [10]	DFF [8]	DFB (Fig. 3)
Theoretical	18.4	19.9	22.2	23.3
Simulation	18.1	19.7	21.9	23.9

Table3: Circuit simulations for different topologies with1.2Vsupply

Load	Resistor [6]	MOS [10]	DFF [8]	DFB (Fig. 3)
Gain (dB)	18.1	19.7	21.9	23.9
NF (dB)	< 3.1	< 2.9	< 3	< 1.8
IIP3 (dBm)	8.2	−3.4	−8.7	−13.1
Power (mW)	5.2	4.9	6.3	5.3
Band (GHz)	0.1 – 10	0.1 – 5.8	0.1 – 5.8	0.1 – 2.2
FOM_1 (mW^{-1})	1.48	2.07	1.98	5.76

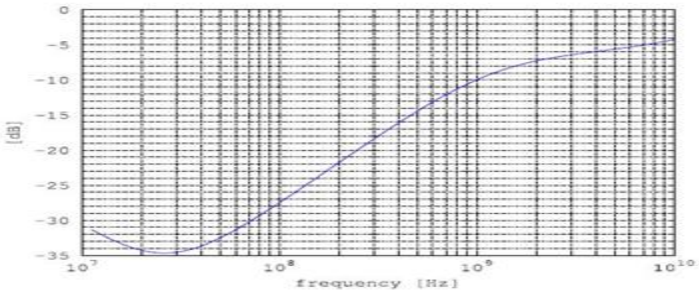

Fig. 4. Simulated S11 parameter for the DFB LNA (Fig. 3).

V. Measurement results

Since the objective of the improved LNA proposed here is to obtain a low area and low power receiver, to demonstrate that this objective can be obtained, we have designed a receiver, which is a modern discrete-time down converter [21,22] for ISM and WMTS bands with the block diagram represented in Fig. 7. Two RF receivers front-end

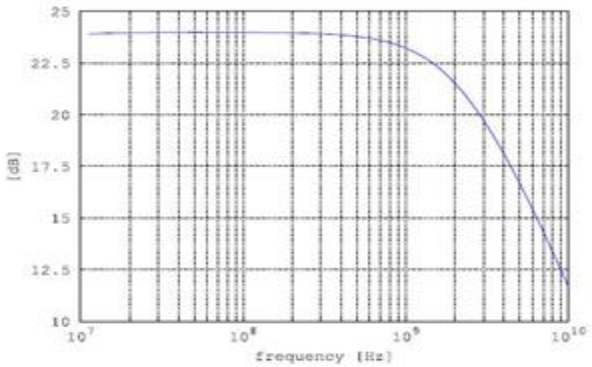

Fig. 5. Simulated gain for the DFB LNA (Fig. 3).

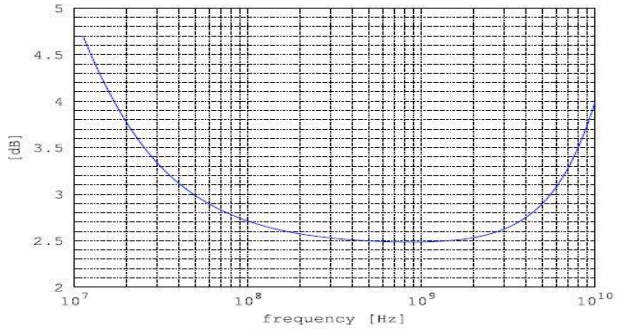

Fig. 6. Simulated noise figure for the DFB LNA (Fig. 3).

circuits were designed and fabricated in the UMC CMOS 130nm technology. For comparison purposes we have implemented two versions of the receiver, one with the DFB LNA (receiver B), and the other with the basic LNA circuit of Fig. 1 using active loads (receiver A). All the remaining blocks are the same in the two receivers.

Table4
Comparison with state-of-the art LNAs. Bold values indicate highlight of the proposed work in comparison with the state-of-the-art

Ref.	Techn. (nm)	Band (GHz)	Voltage gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM_1 (mW^{-1})	FOM_2 (-)
[6][a]	65	0.2–5.2	13–15.6	<3.5	>0	14	0.35	3.45
[15][a]	90	0.5–8.2	22–25	<2.6	−4/−16	42	0.52	0.13
[16][a]	90	0.8–6	18–20	<3.5	>−3.5	12.5	0.65	2.86
[17][b]	90	0.1–1.9	20.6	<2.7	10.8	9.6	1.29	154
[18][b]	130	0.2–3.8	11.2	<2.8	−2.7	1.9	2.11	n.a.
[19][a]	180	0.5–0.9	16	<4.3	-	22	0.17	n.a.
[20][a]	180	0.1–0.9	15	<4.2	-	10	0.34	6.6
[10][a]	130	0.1–2	16.8	<5	>0	4.8	0.67	5.9
This work[b]	**130**	**0.1–2.2**	**21–24**	**2.5–2.7**	**−7.6**	**5.4**	**3.4**	5.85
This work[c]	**130**	**0.1–2.5**	**19.5**	**<5**	**>0**	**5.4**	**0.81**	8

a Measurement results.
b Simulation results.
c Extrapolated results from measurements at 450MHz.

The overall area for each front-end is about 800 x 550 μm^2. The layout and die photo are shown in Fig. 8, where the main blocks and signal pads are highlighted. It is worth mentioning that although the DFB LNA has more area due to the cross-coupled capacitors, this does not affect the overall area, and the full RF front-end circuits have the same area. The other pads are for supply and voltage references as well for external biasing circuits.

All the measurements were done with a spectrum analyzer with a software option for noise figure measurements and a network analyzer for input matching verification (s11). The test board developed for the measurements are shown in Fig.9. The circuits were measured with an RF signal ranging from 250 to 900MHz, which was limited by the internal VCO in terms of frequency. The LNAs performance can be inferred from the relative measurement results; however we can estimate the bandwidth through the 1-port measurement of s11 as shown in Fig.10. For each measurement step, the Internal VCO has to be tuned to convert the RF signal to allow IF of 10MHz. This tuning is performed by adjusting an external trimmer.

We were not able to measure the LNA standalone performance, and therefore, we extrapolate the LNA results, by assuming that the difference from simulation and measurements is at the LNA. This is a worse case assumption that guaranties that the actual performance cannot be worse than the extrapolated result. From the measurements of the proto type with the proposed circuit we have a gain loss of 3.5dB with respect to simulation, which we assume that was only due to the LNA. Thus, the LNA gain is higher than 19.5dB, as indicated in Table4. As for the NF, it has a degradation of 2.7dB, which we attribute to the LNA, since the overall NF is dominated by the first stage, and therefore, we have assumed that the LNA NF is lower than 5dB. Regarding the IIP3, considering the cascaded IIP3, we assume that the IIP3 is dominated by the second stage (i.e., mixer), and therefore we extrapolate a IIP3 above 0dBm for the LNA.

Comparing the two receiver designs, we can observe that the gain increases and the NF decrease for receiver B with the proposed DFB LNA, as shown in Figs. 11and12. The results in terms of linearity are similar (the IP3 of receiver A is 4.9 dB mat 450 MHz, and the IP3 of receiver B is 0.3dBm). However, for biomedical applications the linearity is not a major concern.

VI. Conclusions

In this paper we present a low voltage and low power wide-band balun LNA with DFB for high gain and low NF. A circuit prototype with 1.2V supply is presented in a 130nm CMOS technology, which validates the proposed methodology. The pro-posed circuit is especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands). A receiver for these bands was designed as a demonstrator.

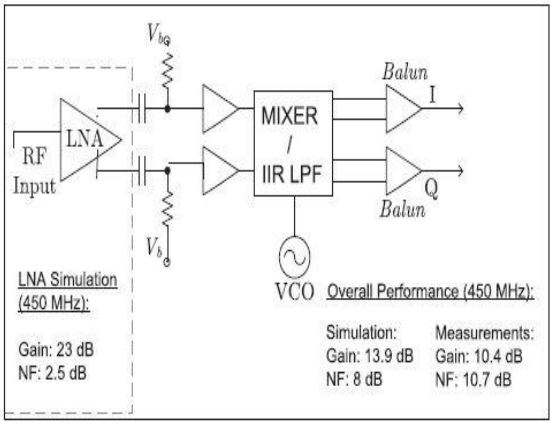

Fig. 7. Block diagram of the implemented receiver.

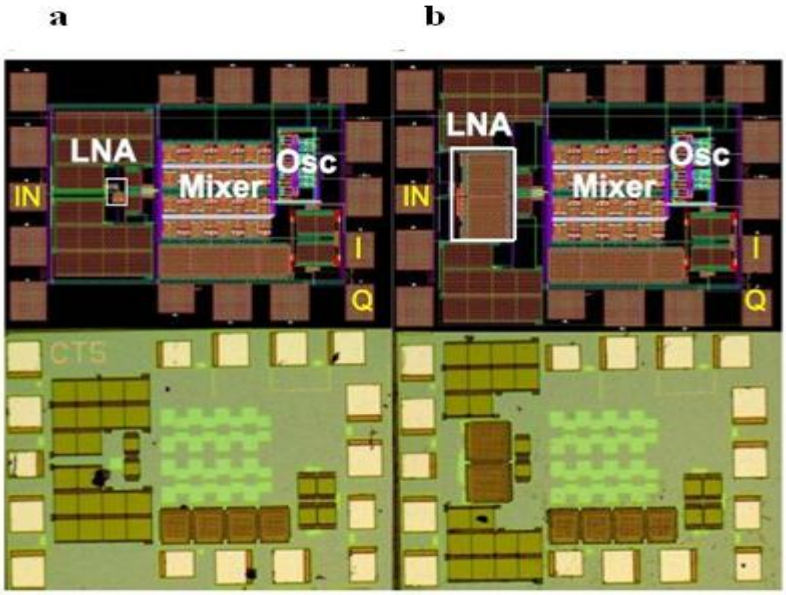

Fig. 8. Die photo and layout:
(a) front-end with the LNA with active loads and
(b) front-endwithDFBLNA.

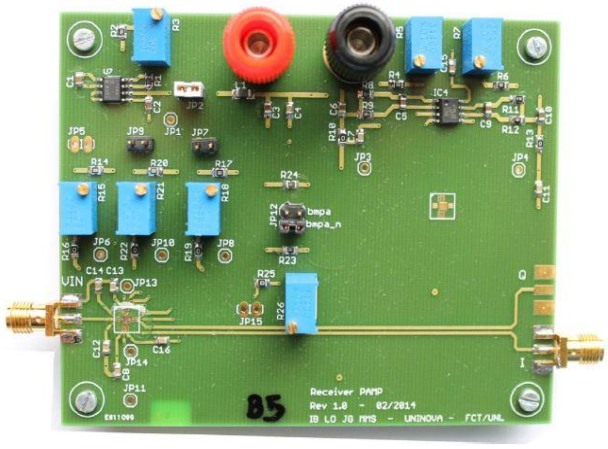

Fig. 9. Prototype board.

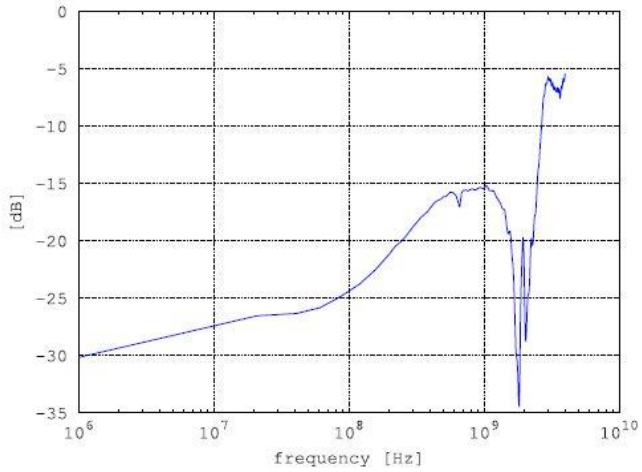

Fig. 10. Measured s11 of DFB NA(receiverB).

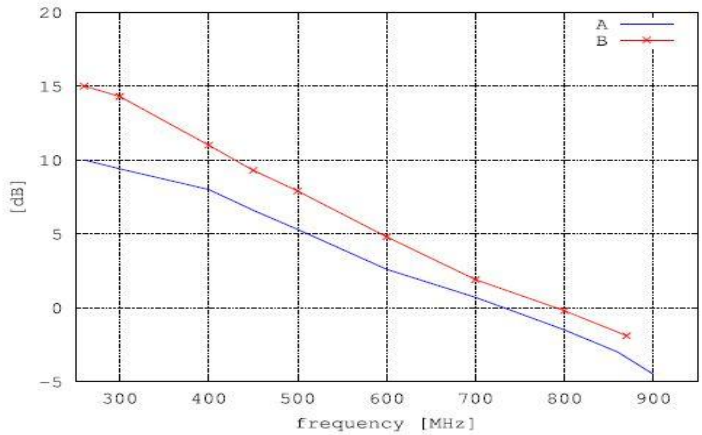

Fig. 11. Front-end gain (receivers A and B)

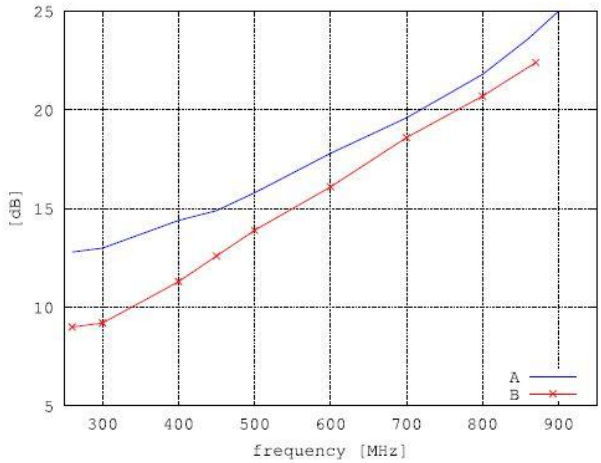

Fig. 12. Front-end NF (receivers A and B).

Measurement results are presented for the receiver using the DFB LNA proposed here and are compared with the results for a receiver using a more basic LNA circuit, with active loads, but without gain boosting. In the band of interest the DFB LNA leads to an improvement of more than 3 dB in the gain, and the NF is reduced by 2 dB for a power consumption of 5.4 mW, when compared with an LNA with active loads, but without feedback.

REFERENCES

[1] K. Iniewski, VLSI Circuits for Biomedical Applications, 1st ed.,Artech House, Inc., Norwood,2008.

[2] B. Razavi, RF Micro electronics, Prentice-Hall, Inc.,New Jersey, 1998.

[3] T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits,2nd ed., Cambridge University Press ,Cambridge,2004.

[4] J.Crols, M.Steyaert, CMOS Wireless Transceiver Design ,Kluwer Academic Publishers, 1997.

[5] F.Bruccoleri, E.Klumperink, B.Nauta, Wide-band CMOS low-noise amplifier Exploiting thermal noise canceling, IEEE J.Solid-State Circuits 39(2)(2004) 275–282.

[6] S.C. Blaakmeer, E.A.M. Klumperink ,D.M.W.Leenaerts ,B.Nauta, Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling, IEEEJ.Solid-State Circuits 43(6)(2008)1341–1350.

[7] I.Bastos, L.B.Oliveira, J.P.Oliveira, J.Goes ,M.M. Silva, Balun LNA with continuously controllable gain and with noise and distortion cancellation, in: 2012 IEEE International Symposiumon Circuits and Systems (ISCAS),2012, pp. 2143–2146.

[8] I.Bastos, L.Oliveira ,J.P.Oliveira ,J.Goes, M.M.Silva, Double feed forward 0.6V LNA with high gain and low noise figure, in:2013 Proceedings of the 20th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), IEEE ,Gdynia, Poland, 2013,pp.235–238.

[9] D. Murphy, H.Darabi, A.Abidi ,A.Hafez, A.Mirzaei, M.Mikhemar, M.-C.Chang, A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications, IEEE J0.Solid-State Circuits 47(12)(2012)2943–2963.

[10] I.Bastos, L.Oliveira, J.Goes, M.Silva, Alow power balun LNA with active loads for gain and noise figure optimization ,Analog Integr .Circuits Signal Process. (2014)1–10.

[11] K.Chew,K.Yeo,S.-F.Chu, Effect of technology scaling on the 1/f noise of deep Sub micron PMOS transistors, Solid-State Electron .48 (7)(2004)1101–1109.

[12] M.Manghisoni, L.Ratti, V.Re,V.Speziali, G.Traversi, Noise characterization of 130nm and 90nm CMOS technologies for analog front-end electronics ,in: 2006 IEEE Nuclear Science Symposium Conference Record, vol.1,IEEE ,2006, pp. 214–218.

[13] D.Linten, L.Aspemyr, W.Jeamsaksiri, J.Ramos, A.Mercha, S.Jenei, S.Thijs,R. Garcia, H.Jacobsson, P.Wambacq, S.Donnay, S.Decoutere ,Low-power 5GHz LNA and VCO in 90nm RF CMOS, in:2004 Symposium on VLSI Circuits – Digest of Technical Papers (IEEE Cat.No.04CH37525), Wider kehrand Associates, 2004,pp.372–375.

[14] R. Brederlow, W.Weber ,J.Sauerer, S.Donnay, P.Wambacq, M.Vertregt, A mixed-Signal design road map, Design & Test of Computers, IEEE18 (6)(2001)34–46.

[15] J.-H.Zhan, S.Taylor, A 5GHz resistive feedback CMOS LNA for low-cost multi-standard applications, in:2006 IEEE International Solid State Circuits Conference – Digest of Technical Papers, IEEE, 2006,pp.721–730.

[16] R.Bagheri, A.Mirzaei, S.Chehrazi, M.E.Heidari, M.Lee, M.Mikhemar, W.Tang, A.A.Abidi, An 800-MHz & 6-GHz software-defined wireless receiver in 90-nm CMOS, IEEE J.Solid-State Circuits 41(12)(2006)2860–2876.

[17] R.Martins, Design of an ESD-protect edultra-wideband LNA in nano scale CMOS for full-band mobile tv tuners, IEEE Trans. Circuits Syst.I:Reg.Pap.56 (5) (2009)933–942.

[18] A. Amer, E.Hegazi, H.Ragai, Alow-power wideband CMOS LNA for WiMAX, IEEE Trans. Circuits Syst.II: ExpressBriefs54(1)(2007)4–8.

[19] J.Xiao, I.Mehr, J.Silva-Martinez, A high dynamic range CMOS variable gain amplifier for mobile DTV tuner ,IEEE J.Solid-State Circuits 42(2)(2007) 292–301.

[20] KefengHan, LiangZou, Youchun Liao, Hao Min,Zhangwen Tang. A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV Tuner applications, in:2008 IEEE Asian Solid-State Circuits Conference,IEEE,2008, pp. 457–460.

[21] Z.Ru, E.A.M.Klumperink, B.Nauta, Discrete-time mixing receiver architecture For rf-samplings of software-defined radio, IEEEJ. Solid-State Circuits 45(9) (2010)1732–1745.

[22] J.R.Custódio, I.Bastos, L.B.Oliveira, J.P.Oliveira, P.Pereira, J.Goes, E.Bruun, A 6.2mW 0.024mm2 fully-passive RF down converter with 12dB gain enhance-Mentusing MOS parametric amplification, Analog Integr .Circuits Signal Process. 75(2) (2013)299–304.

Author Biographies

Mr. K.Raju finished his M.tech in VLSI SYSTEM DESIGN. His area of interest is in the field of analog VLSI. Now presently working as Assistant Professor in ECE dept in G.PULLAREDDY ENGINEERING COLLEGE, Kurnool

.

Mrs. R.Sireesha finished her M.tech in Embedded systems. Her area of interest is in the field of Digital Signal Processing and Digital image processing. Now presently working as Assistant Professor in ECE dept in Brindavan Institute of Technology and Science, KURNOOL

Mr. K.Vijay Kumar finished his M.tech in Communication Signal Processing (C.S.P) in G.Pulla Reddy Engineering College, Kurnool. His area of interest is in the field of Digital Signal Processing and Communications. Now presently working as Assistant Professor in Ravindra College of Engineering For Women Kurnool.