Multiple Single Input Change Vectors for Built-In Self Test (MSIC-BIST)

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ABSTRACT:
Digital circuit's complexity and density are increasing while, at the same time, more quality and reliability are required. These trends, together with high test costs, make the validation of VLSI circuits more and more difficult. In this project we introduce the automatic test pattern generator with multiple single input change (SIC) vectors for post silicon validation schemes. Choosing a best device leads to challenges in various factors, In this paper performs a novel test pattern generator (TPG) for built-in self-test. Our method generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The designed TPG is flexible to both the test-per-clock and the test-per-scan schemes.A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced MSIC sequences have the favorable features of uniform distribution and low input transition density. The performances of the designed TPGs and the circuits under test with 45 nm are evaluated. Simulation results with ISCAS benchmarks demonstrate that MSIC can save test power and impose no more than 7.5% overhead for a scan design. It also achieves the target fault coverage without increasing the test length.

***INDEX TERMS*:** Built in self test,single input change vectors,test pattern generator,Johnson counter.

I. INTRODUCTION

Built-In Self-Test (BIST) techniques used in the VLSI testing. It can be reduce the difficulty and complexity of VLSI testing. The conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. The major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT [1], which can cause excessive power dissipation. Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard et al. analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction.The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno *et al.* provided a low power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in [7] reduces the power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent. However, this dependency implies that non detecting subsequences must be determined for each circuit test sequence. Bonhomme *et al.* [9] used a clock gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia *et al.* [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

Existing System:-

In the existing design a Test Pattern Generator is flexible to both the test-per-clock and the test-per-scan schemes were realized. A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced MSIC sequences have the favorable features of uniform distribution and low input transition density. The performances of the designed TPGs and the circuits under test with 45 nm are evaluated.

Proposed System:-

In the proposed system a sample module is created to do the Built in self test algorithm using automatic test pattern generation also user defined test pattern generation option also we design, The entire hardware is realized as digital logical circuits and the test results are simulated in Modelsim.

II MSIC-TPG SCHEME

A TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple code words.

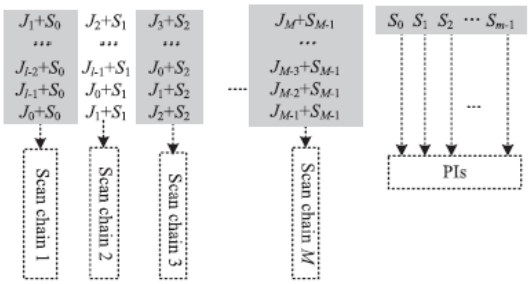

Fig.1 Symbolic representation of an MSIC pattern.

Meanwhile, the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

A. Test Pattern Generation Method

There are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as S(t) = S0(t)S1(t)S2(t), . . . , Sm−1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . . , Jl−1(t).The first clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will bit-XOR with $S = S0S1S2, \ldots, SM-1$, and the results $X1Xl+1X2l+1, \ldots, X(M-1)l+1$ will be shifted into M scan chains, respectively. In the second clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will be circularly shifted as $J = Jl-1\ J0\ J1, \ldots, Jl-2$, which will also bit-XOR with the seed $S = S0S1S2, \ldots, SM-1$. The resulting $X2Xl+2X2l+2, \ldots, X(M-1)l+2$ will be shifted into M scan chains, respectively. After l clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S0S1S2, \ldots, Sm-1$ will be applied to m PIs. Therefore circular Johnson counter can generate l unique Johnson code words through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential de compressor.

B. Reconfigurable Johnson Counter

The different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

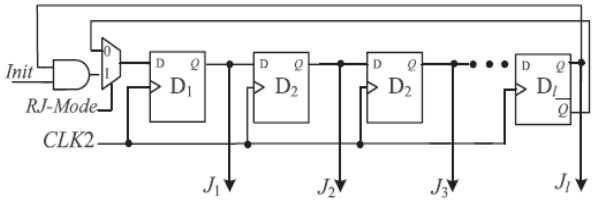

Fig.2 Reconfigurable Johnson counter.

III MSIC SEQUENCES

The proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential de compressor, facilitating hardware implementation. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency.

Scalable SIC Counter: The maximal scan chain length *l* is much larger than the scan chain number *M*, we develop an SIC counter named the "scalable SIC counter." As shown in Fig. 2(b), it contains a *k*-bit adder clocked by the rising *SE* signal, a *k*-bit subtract or clocked by test clock CLK2, an *M*-bit shift register clocked by test clock CLK2, and *k* multiplexers. The value of *k* is the integer of log2*(l − M)*. The waveforms of the scalable SIC counter are shown in Fig. 2(c). The *k*-bit adder is clocked by the falling *SE* signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 2(b), it can operate in three modes.

1)If *SE* = 0, the count from the adder is stored to the *k*-bit subtract or. During *SE* = 1, the contents of the *k*-bit subtract or will be decreased from the stored count to all zeros gradually.
2) If *SE* = 1 and the contents of the *k*-bit subtract or are not all zeros, *M*-Johnson will be kept at logic 1 (0).
3) Otherwise, it will be kept at logic 0 (1). Thus, the needed
1s (0s) will be shifted into the *M*-bit shift register by clocking CLK2 *l* times, and unique Johnson code words will be applied into different scan chains.

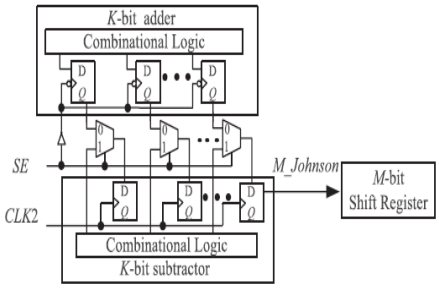

Fig.3 Scalable SIC counter.

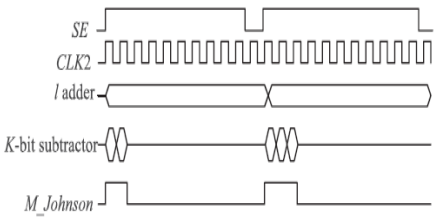

Fig.4 Waveforms of the scalable SIC counter

MSIC-TPGs for Test-per-Clock Schemes: The CUT's PIs X1 − Xmn are arranged as an n ×m SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure is as follows.
1) The seed generator generates a new seed by clocking CLK1 one time.
2) The Johnson counter generates a new vector by clocking
CLK2 one time.
3) Repeat 2 until 2l Johnson vectors are generated.
4) Repeat 1–3 until the expected fault coverage or test length is achieved.

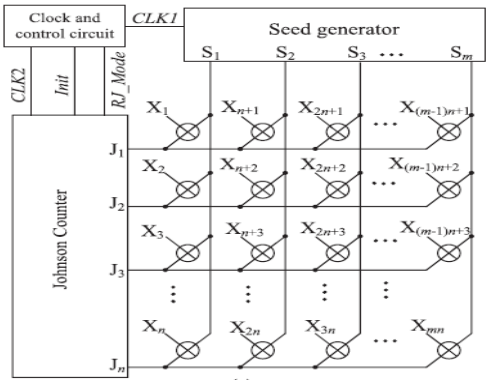

Fig.5 Test-Per-Clock

MSIC-TPGs for Test-per-Scan Schemes: The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 3(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to *M* scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

1) The seed circuit generates a new seed by clocking CLK1
one time.

2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.

3) After a new Johnson vector is generated, RJ_Mode and
Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates *l* code words by clocking CLK2 *l* times. Then, a capture operation is inserted.

4) Repeat 2–3 until 2*l* Johnson vectors are generated.

5) Repeat 1–4 until the expected fault coverage or test length is achieved.

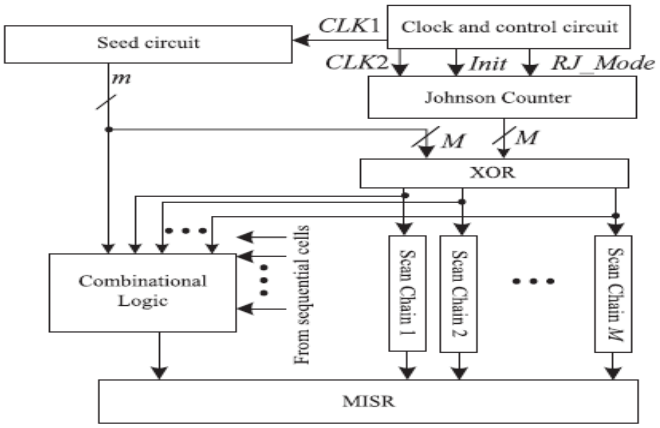

Fig.6 Test-Per-Scan

IV RESULTS

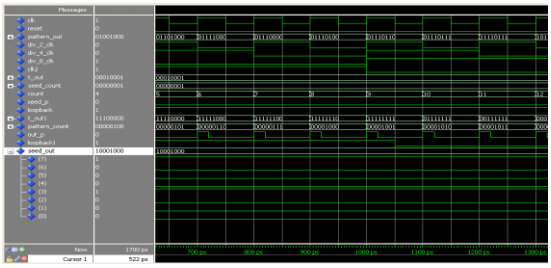

Fig.7 Output For Test Per Clock

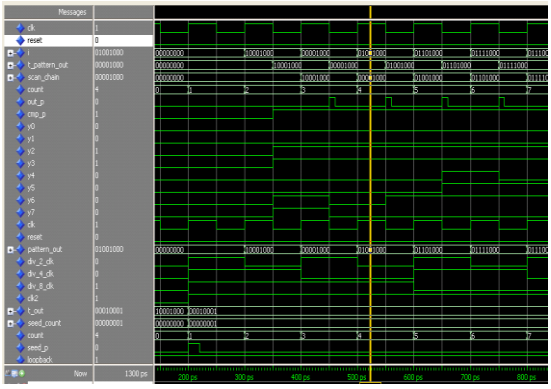

Fig.8 Output for Test per Scan

V CONCLUSION

This paper proposed a low-power test pattern generation method for giving the patterns to the device under test. In this we generate the multiple single input change vectors from the seed produced by conventional 8_bit pseudo random number generator. The power consumption of our proposed system has low because of low transaction behavior of the system. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead. After the generating the MSIC, in this we conduct the validation process on the combinational logic circuit and verified the output.

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