Design Of A Low Power And High Speed 1.5 Bit Stage For Pipeline ADC

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ABSTRACT

The design and the preliminary measurements of a prototype 10 bit pipeline ADC based on 1.5-bit per stage architecture is presented here. For conventional ADCs differential amplifiers dominate the power dissipationin most high-speed pipelined analog-to digital converters (ADCs).We propose a new technique to design Pipeline ADCwith Gm stage as differential amplifier for low power consumption. The gm based amplifier performs a class-AB operation by smoothly changing between a comparator-like semi digital driver and a continuous– time high-gain amplifier according to the input voltage difference.The ADC has been designed with 50nm CMOS technology and achieves the low power upto 1.5 mWand integral nonlinearity within 0.5 LSB and 0.9 LSB, respectively.

Keywords: *Gm-based amplifier, operational transconductance amplifier (OTA), Op-Amp, Pipeline Analog-to-digital converter (ADC),*

I. INTRODUCTION

PIPELINED analog-to-digital converters (ADCs) have lowinput capacitance, high-speed concurrent operation, andhardware complexity that linearly increase with resolution.Accordingly, among various ADC structures, the pipelinedADC is a popular architecture, because it achieves high speedand resolution while maintaining area efficiency and low powerconsumption [6]. As a result, it is a suitable architecture for implementingADCs for video and communication applications.The conventional ADC requires Op-Amp with high power consumption.µcrossing-based circuits [1], dynamic source-followeramplification [2], capacitive charge pump [3], digitally assistedalgorithmic amplifier [4], and ring amplifier [5].These techniques require the additional calibration circuits to reduce thedependency on the stability on parametervariations. The amplifier less technique available in [7] presents a Gm-based amplifier that follows a conventional two-phaseswitched-capacitor circuit. Without any calibration techniqueor digital control, the proposed amplifier achieves a smoothtransition from a comparator-like semidigital operation to acontinuous-time high-gain amplifier whenever needed.

In this paper, we describe the implementation and measurement results of a 10-bit 20 MSamples/s pipelinedADC that uses Gm based amplifier.In order to facilitate and expedite the evaluation of the proposedapproach, we based our design on an existing commercially available pipelinedADC in 0.5µmCMOStechnology [8]. In Section II, we briefly review the architecture of this pipeline ADC. Section III highlights the architecture of Gm based amplifier and section IV gives design of 1.5 bit stage for pipeline ADC architecture. In Section I,we establish the simulation and measuredresults. Finally section VI gives the conclusion and future scope.

II. PIPLINE ADC DESIGN

The pipeline ADC is built of a number of serially connectedconverting stages as shown in Fig. 1. In this work architecturewith 1.5-bit stages is chosen because of its simplicity and immunityto the offsets in the comparator and amplifier circuits [6].The 1.5-bit since generates only three different values coded on2 output bits which are sent to a digital correction block where18 input bits from 9 stages are combined together resulting in10 bits of ADC output.The block diagram of fully differential single stage is shown in Fig. 2. Each 1.5-bit stage consist of two comparators, two pairs of capacitors Cs and Cf , a Gm amplifier, several switches and small digital logic circuit. The stage gain of 2 is obtained setting Cs = Cf .

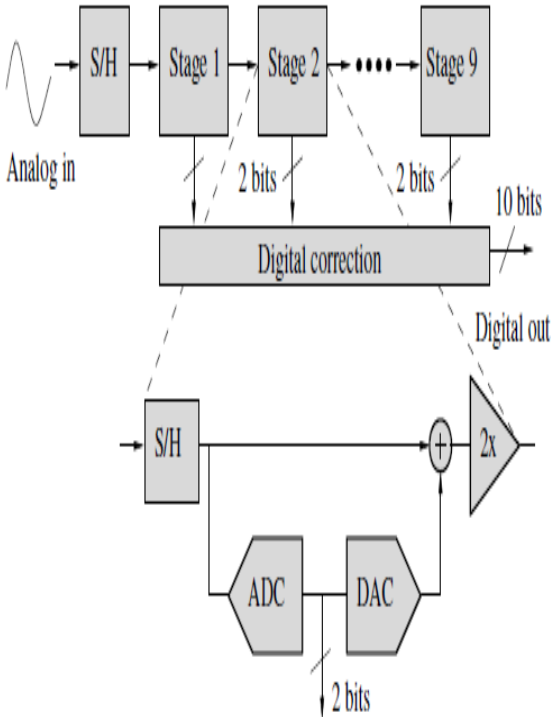

Fig.1 Pipeline ADC architecture

Since the chosen ADC architecture leaves very relaxed requirements on the comparators thresholds (100 mV precision) the comparators are designed as simple dynamic latches. The power consumption block of this ADC is the Gm stage, so a further improved design for this stage is also presented here.

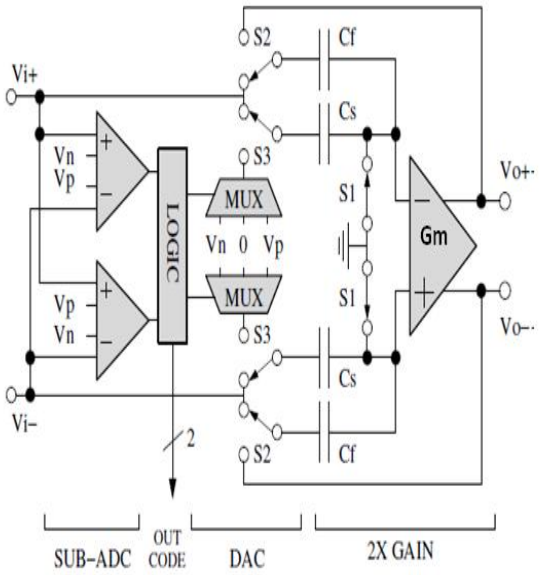

Fig.2 Simplified schematic of a 1.5-bit stage

III. GM-BASED AMPLIFIER

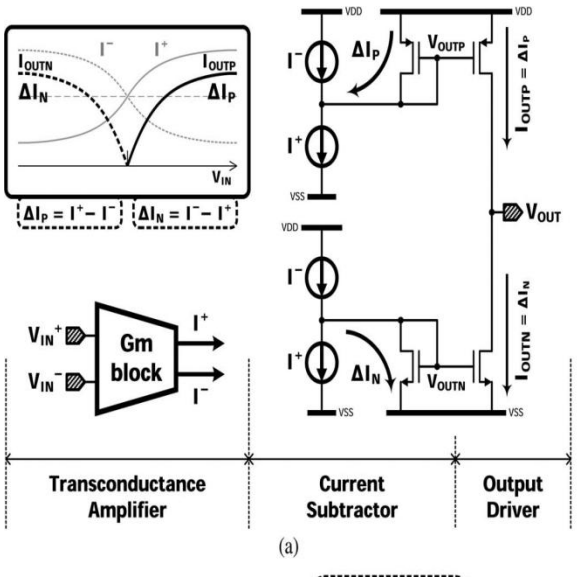

Fig. 3 Concept of the proposed Gm-based amplifier

A new technique to design an Gm based amplifier to reduce the power consumption is proposed in [8]. Fig.3 shows the concept of the proposed Gm-based amplifier, which have a Gm block, a current subtractor stage, and an output driver stage. The amplifier gain is the product of transconductanceGm and the output resistance of the output stage. While Gm does not change much by bias control, the output resistance of a transistor significantly increases as the gate-to-source bias decreases. If the transistors in the output driver are biased to operate in subthreshold region, which almost turns the transistors off, the output resistance approaches to infinity, resulting in an infinite gain of the amplifier.Fig 4 shows the complete circuit structure for Gm based amplifier. The biasing of the output transistors in deep-subthreshold region gives additional benefits. Since the resistance of the output transistors and the load capacitance are much larger than the resistance of the current sources and the parasitic capacitance in the current subtractor, there is no need for an additional frequency compensation scheme. In addition, the proposed amplifier does not require common-mode feedback when used in switched-capacitor circuits driven by nonoverlap-ping two-phase clocks .

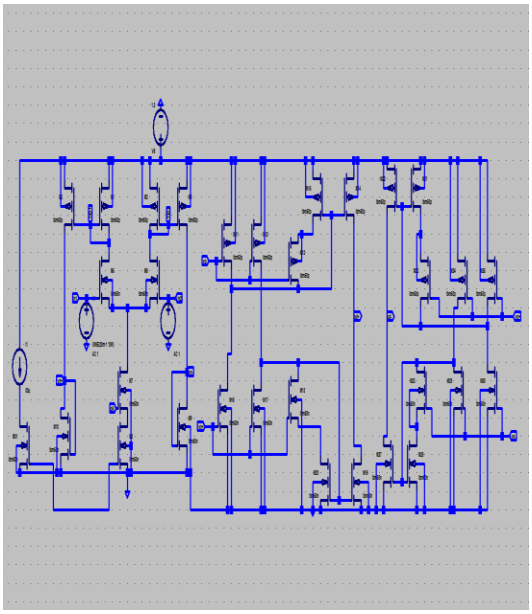

Fig.4 Gm-based amplifier

IV. DESIGN OF 1.5 BIT STAGE FOR ADC

In The complete design of 1.5 bit stage for Pipeline ADC is shown in figure 5. This stage consists the Gm based amplifier, a dynamic comparator and a switched capacitor network with some digital switches. Both the capacitor has the same values.During the sampling phase CP1, the comparator produces a digital output Di. Di is 1 if Vin>Vthand Di is 0 if Vin <Vth, where Vth is the threshold voltage defined midway betweenVref+ and Vref-. During multiplying phase CP2, Cs is connected to the output of the operational amplifier and Cf is connected to either the reference voltage Vref+ or Vref-, depending on the bitvalue Di.

If Di = 1, Cf is connected to Vref+, resulting in the residue(Vout) is :

Vout (i) = 2 Vin(i) –Di.Vref+……(1)
Otherwise, Cf is connected to Vref+, giving an output voltage:
Vout (i) = 2 Vin(i) - Di.Vref-……..(2)

The comparators are the simple dynamic comparators because of less requirements of threshold voltages.

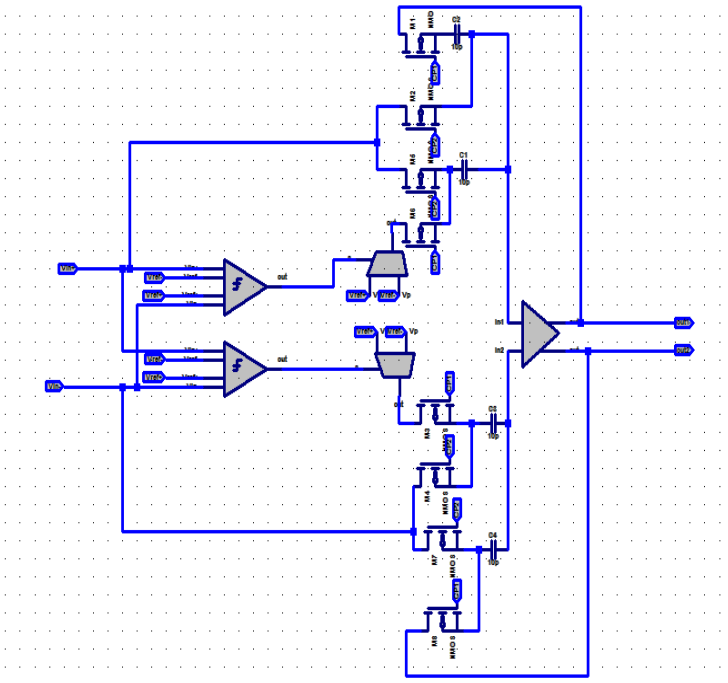

Fig 5 1.5 bit stage design

The 1.5-bit DAC is basically an analog multiplexer controlled by the flash ADC's output. It must be noted that, in the fully differential circuit, the voltage *Vre f* is obtained by swapping the two *Vre f* lines and, therefore it is accurate giving a linear DAC. The SHA provides the analog memory needed for pipelining and does some analog arithmetic. Its output voltage, assuming ideal components, is:

$$Vres \begin{cases} 2\,Vin + Vref for Vin < \dfrac{+Vref}{4} \\ 2Vin for -\dfrac{Vref}{4} < Vin < \dfrac{+Vref}{4} \\ 2Vin - Vref for Vin > \dfrac{+Vref}{4} \end{cases}$$

The input gain of the SHA must be 2 for a proper ADCoperation, but this only happens if the two capacitors *Cs* are perfectly matched and the open-loop gain of the opampis infinite. In our design the sampling capacitance is limited by matching rather than noise because we still have a high voltage swing.

V. SIMULATION RESULTS.

The complete architecture was designed using 50 nm CMOS technology. Fig. 6 shows the frequency response of Gm based amplifier with the Dc gain of 70 dB with unity gain bandwidth of 200MHz. The power delivered by this amplifier is 0.24mW.

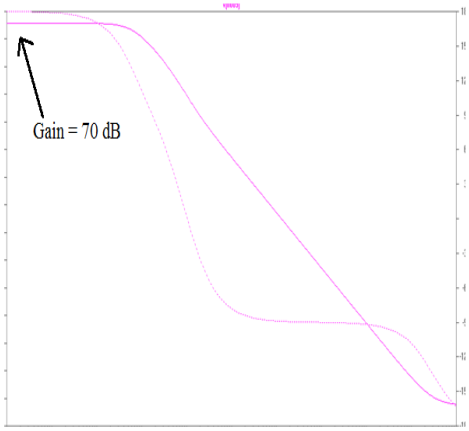

Fig.6 Gain plot for Gm based amplifier

The ADC accepts a full-scale differential input signal of2V peak to peak and has a differential capacitive loading of 3pF. The DNL and INL plots are shown in fig. 7 The measured integral non linearity is 0.6 LSB.The SFDR at 50MHz input is 100dB for the particular stage.The FFT plot for 50MHz samples per second is shown in the fig.8.The simulated results shows that the power dissipated by complete 1.5 bit stage is 1.5 mWat the full conversion speed of 50 MS/s. Table Isummarizes the measured specifications of the prototype ADCs

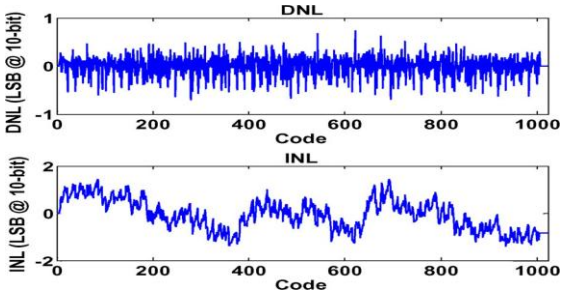

Fig.7 DNL and INL plot for 1.5 bit stage

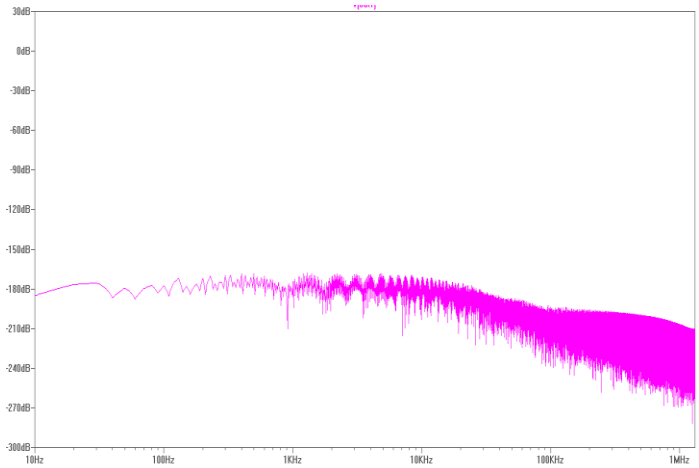

Fig.8 The FFT plot for input frequency of 50MHz

Table I ADC Performance

Parameter	Value
Conversion rate	50 Ms/s
Input range	2 V
Amplifier gain	70 dB
Power supply	1.8V
Power consumption	1.5mw
SFDR (50MHz input)	100dB

VI. CONCLUSION

This paper proposes a new pipeline ADC architecture, which takes advantage of a large stage resolution in the first stage of the pipeline. This architecture shows the low power consumption in the pipeline concept. The prototype ADC demonstrates the ability of this new architecture.The architecture achieves a calibration-free, highresolution,moderate-speed, area-efficient and power-efficientADC design, which is difficult to achieve with traditional ADCs.

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