Comparative study of capacitance of Nano-Scale and Pico-scale-MOSFET

[1] Kaushik Chandra Deva Sarma, [2] Janmoni Borah, [3] Dhruba Kr. Mandal, [4]Ajay chetry, Sanjeeb Kumar Deb Roy, Bhaskar Hazarika

(Dept. of Electronics and Communication Engineering)
Central Institute of Technology Kokrajhar, BTAD, Assam

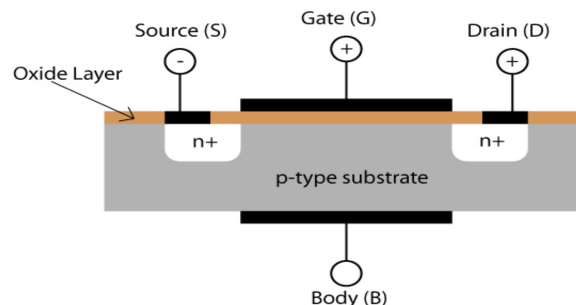
ABSTRACT

As CMOS technology dimensions are being aggressively scaled to reach a limit where device performance must be assessed against fundamental limits, pico scale device modeling is needed to provide innovative new MOS devices as well as to understand the limits of the scaling process. This paper presents a comparison between nanoscale and pico scale MOSFETs from the viewpoint of device physics. The MOS capacitance for different dielectric is compared for device dimensions in nanometer and pico meter using MATLAB.

Keywords: *Channel length, Gate oxide thickness, Gate capacitance, dielectric constant, nanometer, Pico meter, Threshold voltage.*

I. INTRODUCTION

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. The MOSFET behaves as a capacitor as there is a dielectric layer in between semiconductor and metal.



The gate of the Mos is a good capacitor. Its capacitance attracts the Charges to invert the channel. So, Higher the capacitance higher will be drain current.

Capacitance Comparison

We have

$Cg = CoxWL$

Cg = Gate capacitance, W= width of dielectric,

Cox=oxide capacitance, L = Length of dielectric

We have,

$Cox = \epsilon ox/ tox$

tox = Thickness of dielectric .

$\epsilon ox= K \epsilon 0$

$\epsilon 0$= permittivity in free space

k = Dielectric constant

Materials	Dielectric constant
1. Acetamide	4
2. Acetic acid	4.1
3. Anisole	4.3
4. Amylamine	4.6
5. Benzyl benzoate	4.8
6. Benzyl acetate	5
7. Boronyl chloride	5.2
8. Bromohexane	5.8
9. Amyl Bromide	6.3
10. Ammonium chloride	7
11. Apatite	7.4
12. Decanal	8.1
13. Ethyl carbonate	14.2

We have k (Sio2) = 3.9

And the value of thickness and width of the have taken up to 5 nanometer.

Let us change the value of dielectric constant (K):

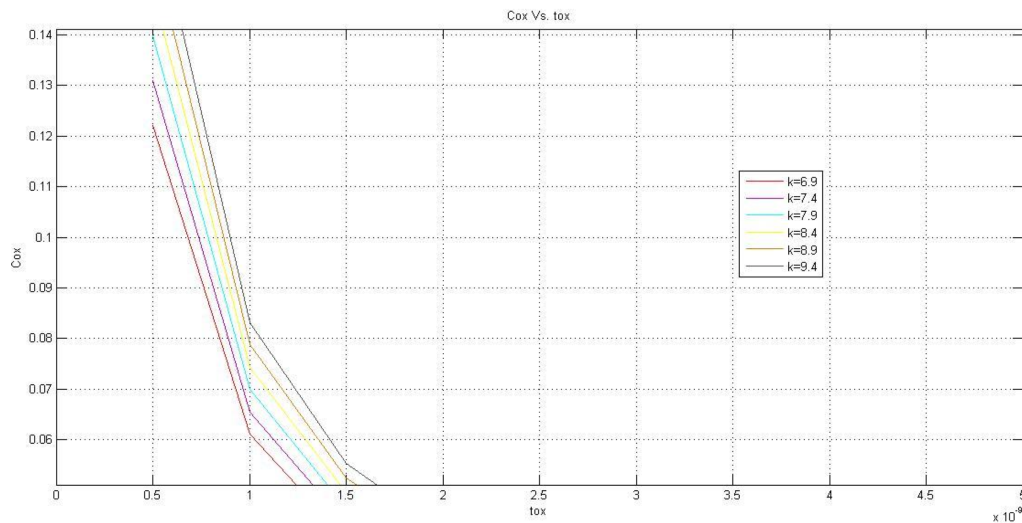
1) If $k < 3.9$, Threshold voltage Increases.
2) If $k > 3.9$, Threshold voltage Decreases.

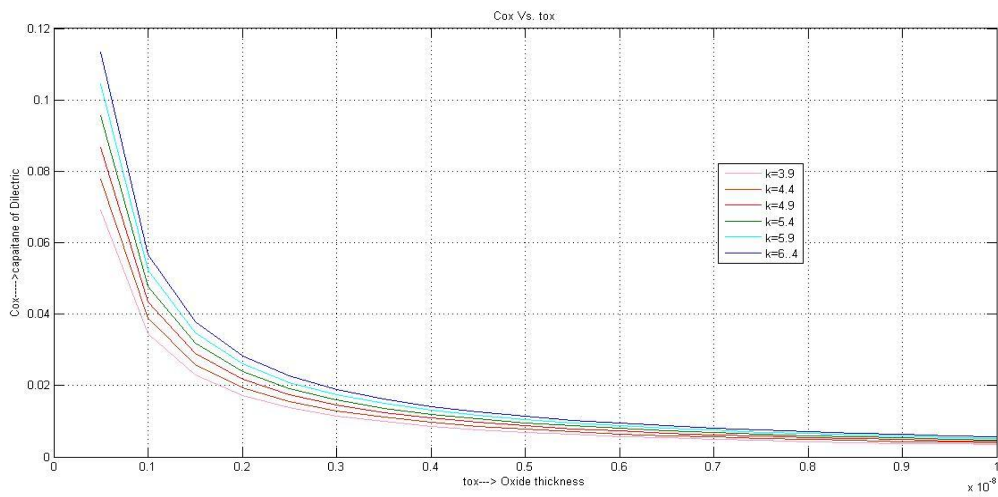
So changing the value of k where $k > 3.9$

And take the value of W, L in bellow 5 nanometer.

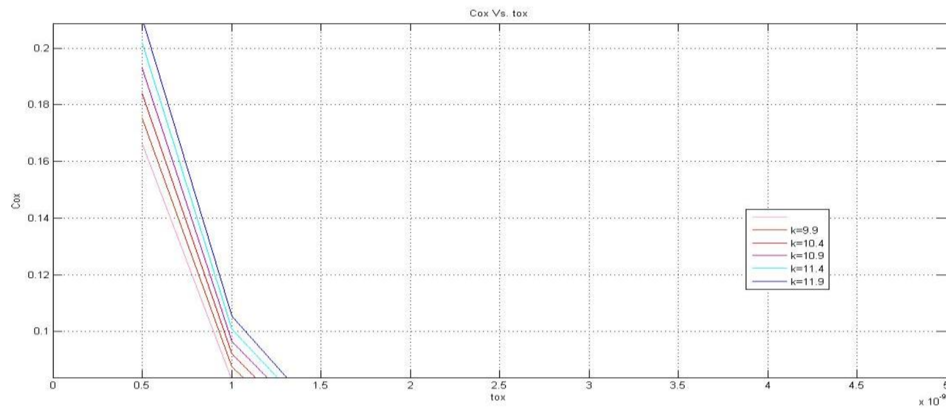
If we plot Cox Vs Tox

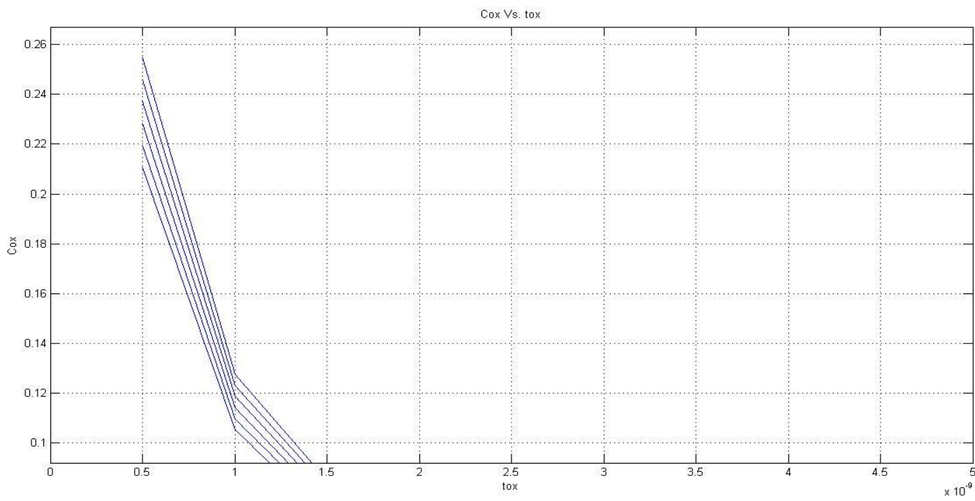
1) Taking the value of Tox in Nanometer





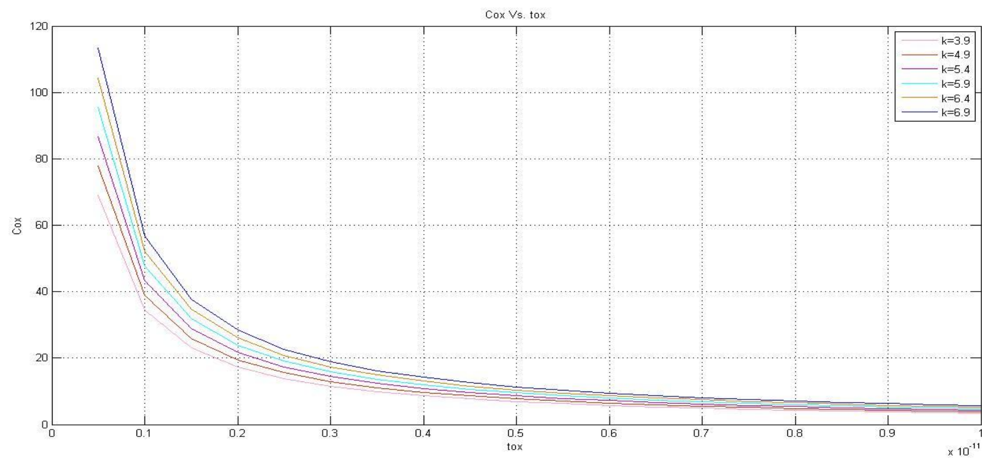
k=3.9 to 6.4
k=6.9 to 9.4



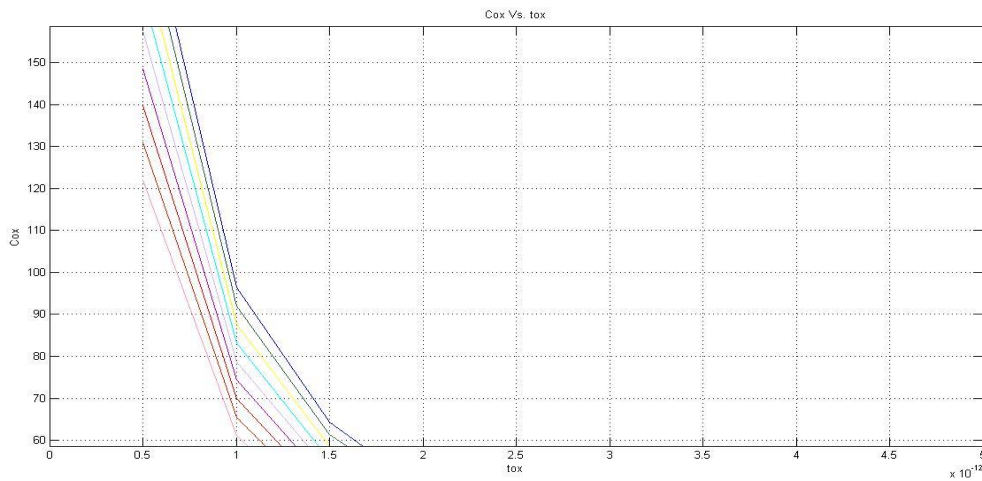


k=9.9 to 11.9
k=11.9 to 14.4

2) Taking the Tox in Picometer



K=3.9 to 6.9
K=7.4 to 11.9

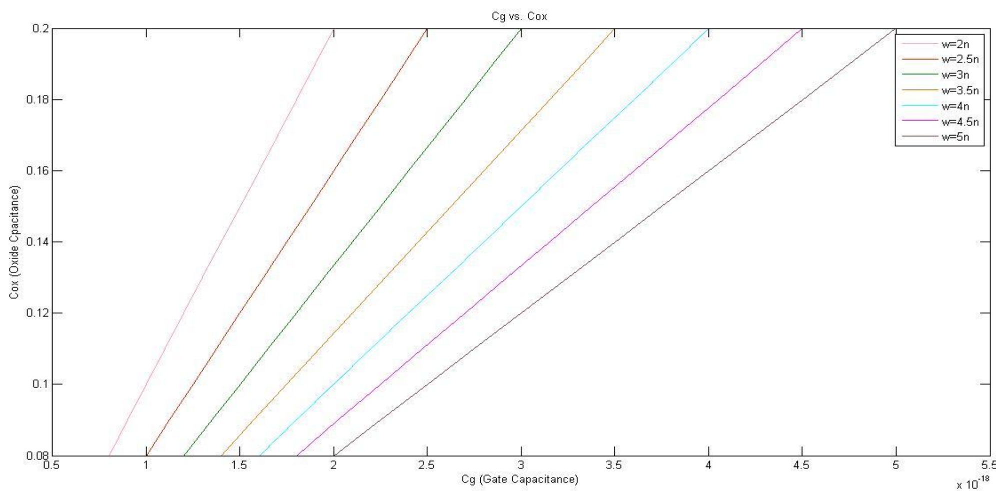


To study Cg vs. Cox

We have

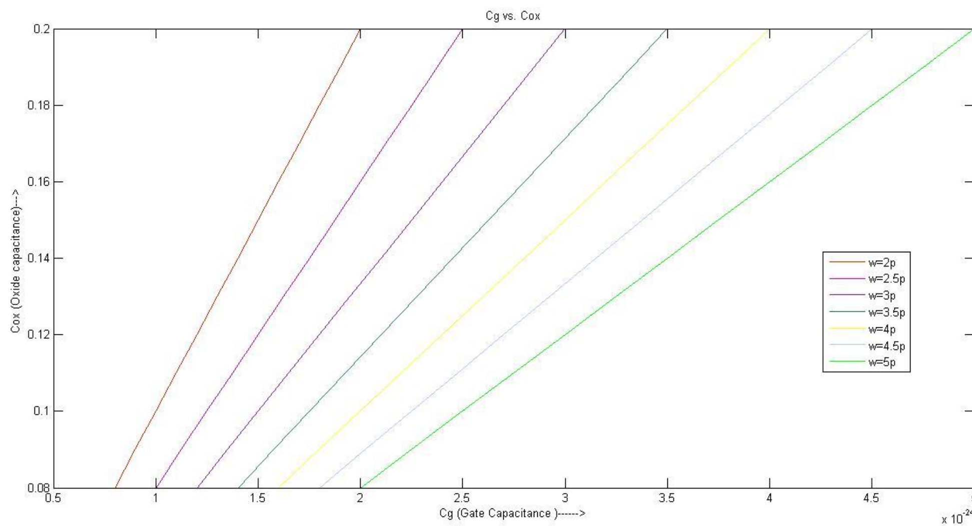
Cg = Cox W L

From above plotted graphs, using Cox= 0.08:0.01:0.20;



Case 1: taking W in nanometer

W=2 to 5nm



Case 2: W in picometer

W=2 to 5 pm

CONCLUSION

There are a number of issues in scaling MOSFET devices, particularly for the sub-100 nm technology evolution. The most critical issue is the gate dielectric, because very thin gate oxides are required for sub-100 nm generations. For such thin oxides, gate leakage current due to direct tunneling becomes unacceptably large. In order to decrease the leakage current due to tunneling, the physical thickness of the dielectric must increase, while the equivalent oxide thickness must continue to be reduced. Use of alternate gate materials with dielectric constant higher than that of silicon dioxide is the leading projected solution to reduce the gate leakage current to more tolerable levels. Therefore, modeling of the thin oxide related issues, such as gate direct tunneling current, gate capacitance, and capacitance reconstruction are crucial for further gate oxide scaling.

ACKNOWLEDGEMENTS

On the very outset of this report, we would like to extend our sincere & heartiest obligation towards all the personages who have helped us in this Endeavour. Without their active guidance, help, co-operation & encouragement, we would not have made headway in the project.

We would also like to thank **Mr. Arindum Mukherjee (HoD i/c, Dept of ECE, CIT Kokrajhar)**, to give us the chance to do this work and all the staff members of ECE dept. for their motivation, guidance and support throughout the project First and foremost, we would like to thank **Mr. Haradhan Chel (Asst. professor, Dept of ECE, CIT Kokrajhar)** who instead of his busy schedule, always guided us in the right direction. We were privileged to experience a sustained enthusiastic and involved interest from his side. This fuelled our enthusiasm even further and encouraged us to boldly step into what was a totally dark and unexplored expanse before us. He always fuelled our thoughts to think broad and out of the box.

REFERENCES

[1] “Modeling of nanoscale mosfets”ChanghoonChoi ,April 2002
[2] H. Iwai, “Current Status and Future of Advanced CMOS Technologies:Digital and Analog Aspects,”1998
[3] R. Viswanathan, and et al.,“CMOSscaling into nanometer regime,”Proceedings of IEEE, Apr. 1997.
[4] “International TechnologyRoadmapfor Semiconductors 2000 Edition,”2000.
[5] E. J. Lerner, “The End of the Road for Moore’s Law,” Journal of IBM research, 1999.
[6] P.A.Packan,“Pushing the Limits,” Sep. 1999
[7] C. Fiegna and A. Abramo “Analysisof Quantum Effects in Nonuniformly Doped MOS Structures,” IEEETrans. Electron Devices, Apr. 1998.
[8] H. Iwai, “CMOS Technology – Year2010 and Beyond,” IEEE J. of Solid-StateCircuits, Mar. 1999.