Efficient Model for OFDM based IEEE 802.11 Receiver with Autocorrelation technique And CORDIC algorithm

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ABSTRACT:

To achieve compact spectral utilization with utmost efficiency in OFDM based WLAN receiver, Autocorrelator and CORDIC algorithm is used. This paper deals with simulation of these algorithms using Verilog HDL. An Autocorrelator takes care of frame synchronization, time synchronization, frequency synchronization by autocorrelating the received signal. CORDIC is an iterative trigonometric algorithm that performs vector rotations with one additional bit of accuracy for each iteration. It is used to estimate frequency offset by calculating the phase of the maximum correlating signal.

***Keywords* -** *Autocorrelator, CORDIC, frequency offset, Iteration, Synchronization.*

I. INTRODUCTION

During recent years the need for mobile broadband communications has increased rapidly placing new demands for the wireless local area networks (WLANs). To answer these needs, the European Telecommunications Standards Institute (ETSI) is working on HIPERLAN (HIgh PERformance LAN) standards. The HIPERLAN/2 architecture is easily adapted and integrated with a variety of fixed networks. It has a very high transmission rate up to 54 Mbit/s in 5GHz band. This is achieved by making use of a modularization method called Orthogonal Frequency Digital Multiplexing (OFDM) [1]. The basic idea of OFDM is to transmit broadband, high data rate information by dividing the data into several interleaved, parallel bit streams, and let each bit stream modulate a separate subcarrier [1].

The property of orthogonality allows simultaneous transmission on a lot of sub-carriers in a tight frequency space without interference from each other. This acts as an advantage in OFDM [3][4][5].Therefore, OFDM is becoming the chosen modulation technique for wireless communication. OFDM is particularly efficient in time-dispersive environments. With the help of OFDM, sufficient robustness can be achieved to provide large data rates to radio channel impairments. OFDM requires extensive use of Autocorrelator and CORDIC. In this paper we will give the implementation details needed by the Hiperlan 2 standard, but most of the work can be generalized to the IEEE standards since physical layer in both three standards are similar (a common synchronization solution is found in [2]).

The paper is organized as follows. In section II we describe the WLAN Receiver structure and its modulation technique is discussed. In section III and IV we discuss about Autocorrelator and CORDIC blocks respectively. The simulation results of these blocks are discussed in section V. Finally conclusions are drawn in section VI.

II. WLAN RECEIVER MODEL

2.1. Modulation Scheme

A combination of modulation and multiplexing constitutes the orthogonal frequency division multiplexing, in other words OFDM. Modulation is the process of transforming the carrier into waveforms suitable for transmission across channel, according to parameters of modulated signal [6]. A key feature of the physical layer is to provide several physical layer modes with different coding and modulation schemes, which are selected by link adaptation. BPSK, QPSK and QAM are the supported subcarrier modulation schemes. The most useful type of modulation for OFDM (orthogonal frequency division multiplexing) is Quadrature amplitude modulation (QAM). QAM changes phase and amplitude of the carrier, and it is a combination of amplitude shift keying (ASK) and phase shift keying (PSK).

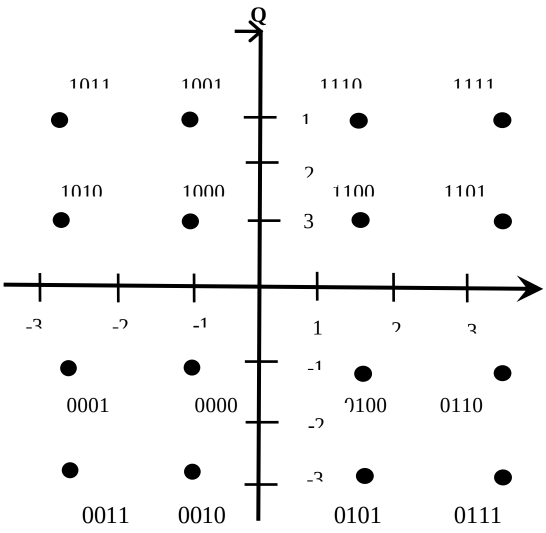

Figure 1. QAM Constellation

2.2 *WLAN Receiver structure*

Fig 2 shows the block diagram of the WLAN transceiver. The IF-stage has been designed to upconvert the transmitted signal at a frequency of 20 MHz, and to downconvert from a frequency of 45 MHz. In WLAN standards the base band OFDM signal is built using a 64-point IFFT.

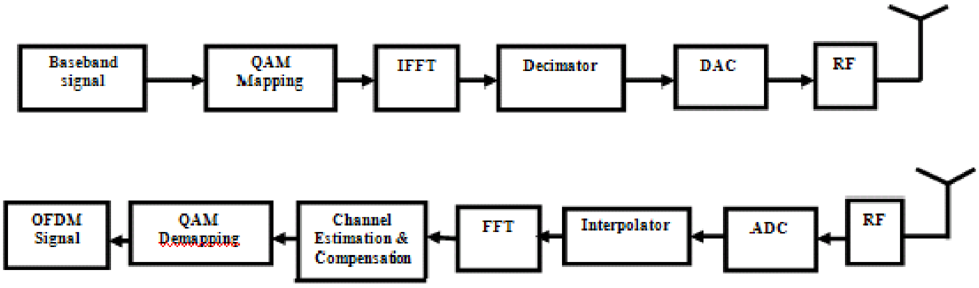

Figure 2. WLAN Transceiver

After down-conversion the following stages are applied to the base-band signal (see Figure 2): timing synchronization, coarse and fine carrier frequency offset (CFO) estimation and correction, FFT-based OFDM demodulation, channel estimation and compensation.

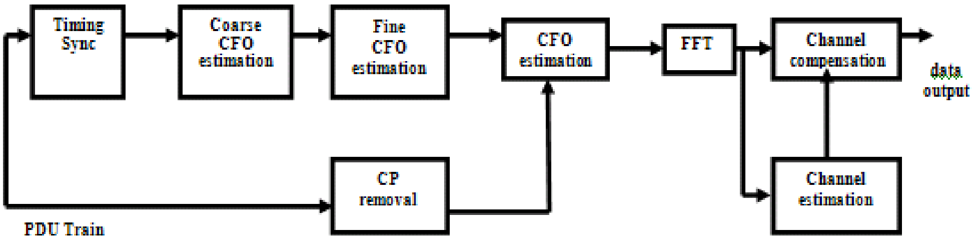

Figure 3. Receiver Structure

In WLAN systems, synchronization and channel compensation is done by using a preamble. So, in Hiperlan/2 the access point transmits a broadcast preamble that is used by mobile terminals (MT) to perform synchronization for both time, frame and frequency, automatic gain control (AGC), and channel estimation. Therefore, the synchronization phase in an MT can be divided in three parts: broadcast preamble detection; time synchronization, that consists of estimating the sample when the OFDM symbol starts and carrier frequency offset (CFO) estimation.

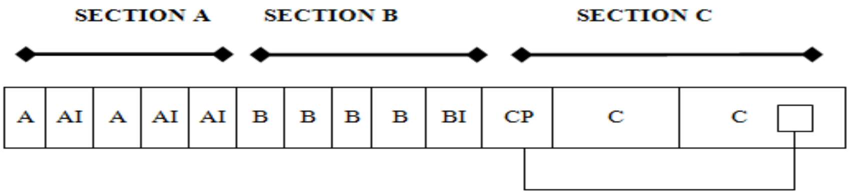

Figure 4. Preamble Structure

In this preamble ,section A is used for AGC and frame detection, section B is intended for time synchronization and coarse CFO estimation and section C can be used for fine CFO estimation and channel estimation.

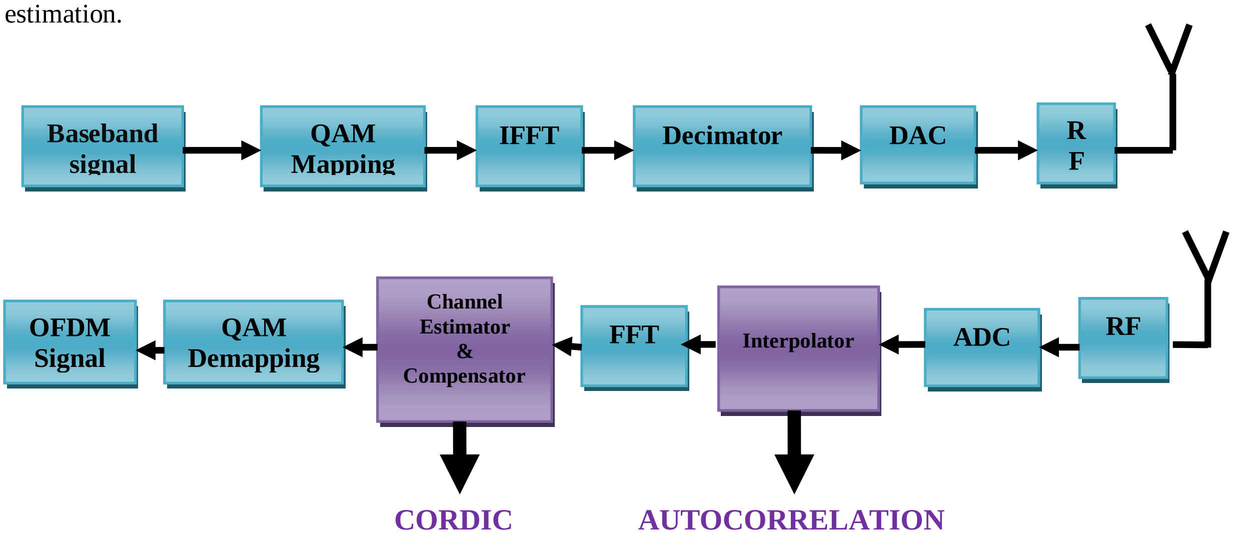

Figure 5. Block diagram of the proposed model

III. AUTOCORRELATION

Autocorrelation is a measure of how well a signal matches a time shifted version of itself, as a function of the amount of time shift. Autocorrelation of a random signal is also be described as correlation between values of the same signal at different points in time. Therefore, autocorrelation can be used to distinguish repeating patterns in signals. A quite basic application of autocorrelation is determining tempo for musical beat or pitch detection. It is a measure of similarity between a data set and a shifted copy of the data as a function of shift magnitude**.** Correlation analysis is used to find periodic patterns in noisy data, characterize similarity patterns in data compression, and measurement of spatial resolution of an image receptor with uniform white noise as the input. For medical imaging a major use of autocorrelation is for the measurement of film and screen spatial resolution[7].

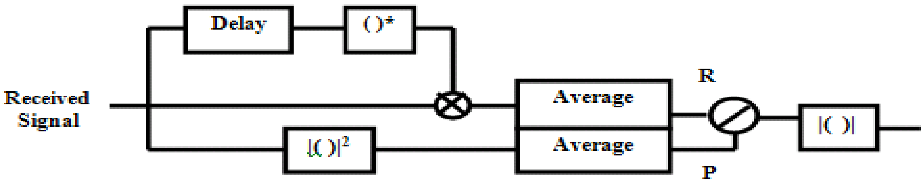

Figure 6. Block diagram of Autocorrelator

The autocorrelation function will be designated as Cx(Δ),

where $Cx(\Delta) = E\{I(x)\, I(x+\Delta)\}$ (1)

This equation tells that the autocorrelation of the any signal is the expected value of product of the same signal with delayed version of itself.

3.1 Autocorrelation based detection

Detection is based on the value of the autocorrelation coefficient of the received signal. In this detection method, the system is identified by the time delay value (Td), which should provide a nonzero autocorrelation value, if the received signal is from a particular radio system and about 0, if the received signal is noise. The decision making is based on the knowledge of statistical distribution of the autocorrelation coefficient. Once the value of the autocorrelation coefficient is computed, the decision can be performed so that a predefined false alarm rate specification of detection is fulfilled.

Autocorrelation-based detection can effectively detect PU signals under the noise floor, and is able to identify specific OFDM-based signaling systems. The implementation is relatively simple, since no FFT is done to the input signal. This limits the detection to the baseband frequency, but resource gain from omitting a FFT is significant for a low power implementation.

IV. CORDIC (COORDINATE ROTATION DIGITAL COMPUTER)

The CORDIC means Coordinate Rotation Digital Computer algorithm was developed in 1959. It rotates the vector, step by step, with a given angle. Additional theoretical work has been done in 1971. The main principle of CORDIC are calculations based on shift registers and adders instead of multiplications, what saves much hardware resources.It is used for polar to rectangular and rectangular to polar conversions and also for calculation of trigonometric functions, vector magnitude and in some transformations, like discrete Fourier transform (DFT) or discrete cosine transform (DCT).

The CORDIC is hardware efficient algorithms for computation of trigonometric and other elementary functions that use only shift and add to perform. The CORDIC set of algorithms for the computation of trigonometric functions was designed by Jack E.Volder in 1959 to help building a real time navigational system for the B-58 bomber. Later, J. Walther in 1971 extended the CORDIC scheme to other functions. The CORDIC method of functional computation is used by most calculators (such as the ones by Texas Instruments and HP) to approximate the normal transcendental functions.

Depending on the configuration, the resulting module implements pipelined, parallel pipelined, word serial, or bit-serial architecture in one of two modes, rotation or vectoring. In rotation mode, the CORDIC rotates a vector by a certain angle. This mode is used to convert polar to Cartesian coordinates. For example consider the multiplication of two complex numbers x+jy and (cos(θ) +jsin(θ)). The result u+jv , can be obtained by calculating the final coordinate after rotating a 2x2 vector $[x\ y]^T$ through an angle (θ) and then scaled by a factor r. This is achieved in CORDIC via a three-stair procedure such as angle conversion, vector rotation and scaling.

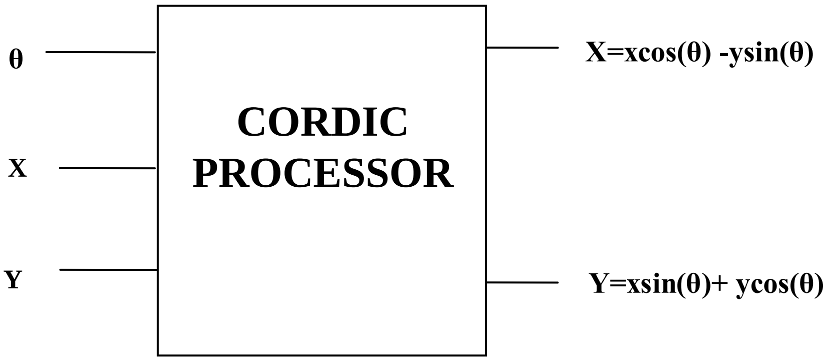

Figure 7. Block diagram of CORDIC Processor

The circular cordic rotation is shown in fig 7.

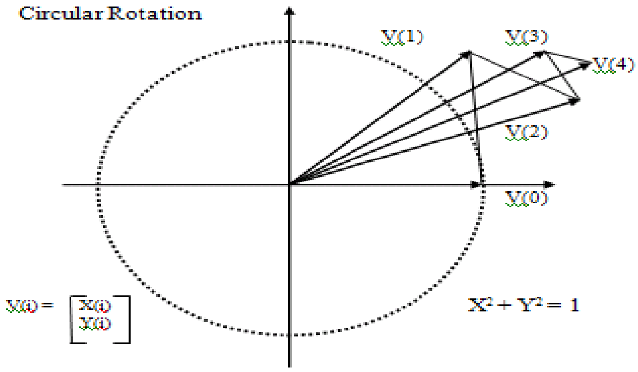

Figure 8. Circular CORDIC rotation

CORDIC is based on the common rotation equations.The vector rotation is given as

$$x' = x\cos(\varphi) - y\sin(\varphi) \tag{2}$$

$$y' = y\cos(\varphi) + x\sin(\varphi) \tag{3}$$

$$x' = \cos(\varphi)[x - y\tan(\varphi)] \tag{4}$$

$$y' = \cos(\varphi)[y + x\tan(\varphi)] \tag{5}$$

$$x_{i+1} = \cos(\tan^{-1}(\pm 2^{-i}))\cdot[x_i - y_i \cdot d_i \cdot 2^{-i}] \tag{6}$$

$$y_{i+1} = \cos(\tan^{-1}(\pm 2^{-i}))\cdot[y_i + x_i \cdot d_i . 2^{-i}] \tag{7}$$

$$x_{i+1} = K_i \cdot [x_i - y_i \cdot d_i \cdot 2^{-i}] \tag{8}$$

$$y_{i+1} = K_i \cdot [y_i + x_i \cdot d_i \cdot 2^{-I}] \tag{9}$$

$$z_{i+1} = z_i - d_i \cdot \arctan(2^{-i}) \tag{10}$$

where $K_i = \mathrm{Cos}(\mathrm{Tan}^{-1} 2.\exp(-i)) = 0.60725$ and $d_i = \pm 1$

So to reach an expected angle, a series of iterations are required to be performed and in this design the number of iterations are 8 and in every iteration the new values of x, y and z depend upon the previous values of the same.

According to [8] [9], the CORDIC processor can be configured to work as circular, hyperbolic and linear rotations for both vectoring and rotational modes. The circular vectoring mode is used to calculate coarse Carrier Frequency Offset (CFO) estimation and fine CFO estimation. The circular rotation mode is used to correct coarse CFO of the broadcast preamble, and to correct received section C and received OFDM symbols. The linear vectoring mode is used to calculate the division in the channel estimation stage.

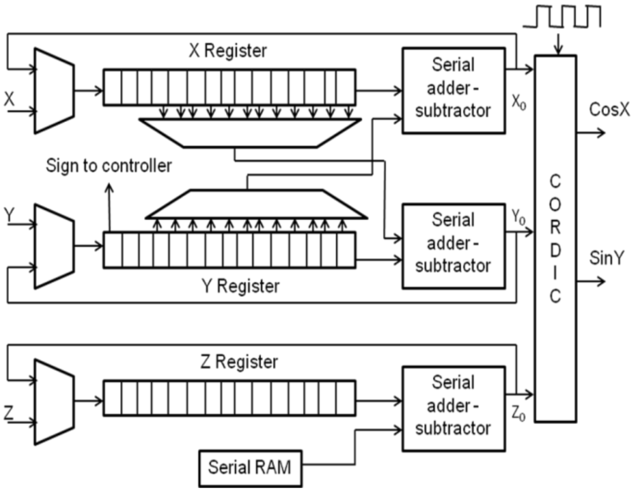

Figure 9. Operation of CORDIC Algorithm

V. SIMULATION RESULTS OF THE PROPOSED MODELS

The proposed model of both Autocorrelator and CORDIC algorithm have been coded in Verilog HDL, synthesized using Xilinx ISE 9.2i which also specifies the number of hardware required. Table I shows the hardware usage of the Autocorrelator.

5.1 Results of Autocorrelator block

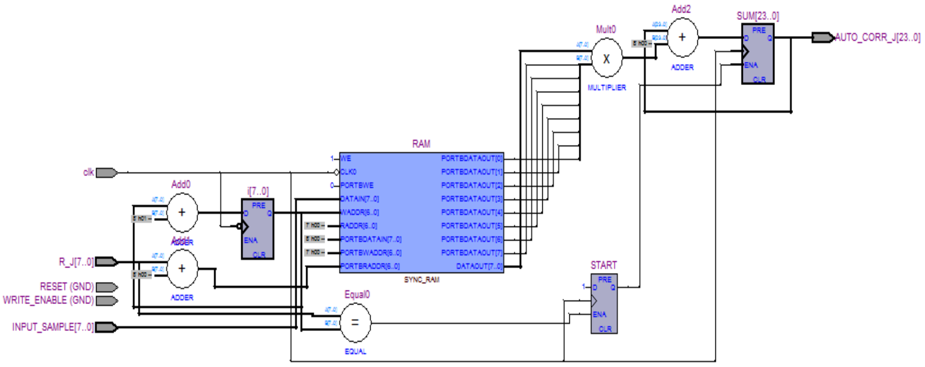

Figure 10. RTL Schematic of Autocorrelator

The RTL schematic of proposed autocorrelator block is shown in fig 9. The proposed autocorrelator block is designed using various units like Adders, Subtractors, RAM, Flipflops, Multipliers. The main aim of autocorrelator block is done by the adder and subtractor unit. Adder and subtractor unit takes care of correlation process. RAM is used for storage purpose. It is used for storing both input sample and the delayed version of itself.

TABLE I: HARDWARE USAGE OF AUTOCORRELATOR

LOGIC UNIT	NUMBER REQUIRED
RAM	**2**
Multiplier	**1**
Adder/Subtractor	**2**
Counter	**2**
Accumulator	**1**
Register	**2**
Comparator	**1**

The maximum period and the maximum frequency of the proposed design is **21.792 ns** and **45.888 MHz.** The delay which is obtained in the proposed model is **10.896 ns** and also the offset of the model is **15.492 ns.**

TABLE II: RESOURCE USAGE OF AUTOCORRELATOR

LOGIC ELEMENTS	UTILISED	AVAILABLE
Number of slice flipflops	**64**	**1920**
Number of 4 input LUTs	**366**	**1920**
Number of occupied slices	**210**	**960**
Total number of 4 input LUTs	**387**	**1920**
Number of bonded IOBs	**43**	**66**
Number of BUFGMUXs	**1**	**24**
Number of multiplier	**1**	**4**
Average fanouts of nonclock nets	**5.43**	**-**

5.2 Results of CORDIC Algorithm

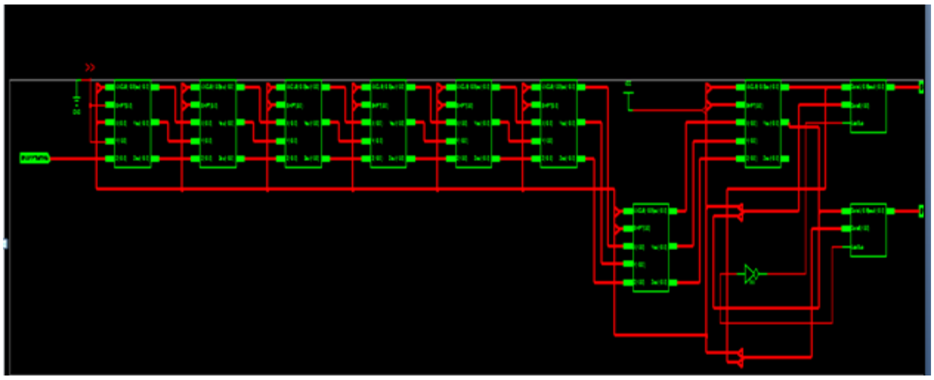

Figure 11. RTL schematic of CORDIC Algorithm

The fig 10 shows the RTL Schematic of CORDIC Algorithm. This model consists of **eight iterator blocks, adders/subtractors, comparators, multipliers and logic shifters**. Each iterator block sequentially provides the output. The output of previous iterator block is taken as the input of next iterator block and process goes on sequentially like this upto eight iterations.

TABLE III: HARDWARE USAGE OF AUTOCORRELATOR

HARDWARE	NUMBER REQUIRED
Multiplier	4
Adder/Subtractor	32
Comparators	52
Logic shifters	40
IO buffer	48
IBUF	16
OBUF	32
IOs	49

The delay for the proposed CORDIC Algorithm is **66.321ns**. The total memory usage which obtained in this model is **297012Kilo bytes.** The total real time to Xst completion is **31s.** The total CPU time to Xst completion is **31.24 s.**

TABLE IV: RESOURCE USAGE OF CORDIC ALGORITHM

LOGIC ELEMENTS	USED	AVAILABLE
Number of slice flipflops	542	960
Number of 4 input LUTs	1031	1920
Number of bonded IOBs	48	66
Number of multiplier	4	4

VI. CONCLUSION

The Proposed model concludes that the performance of the WLAN receiver has been enhanced by means of Autocorrelator and CORDIC Algorithm.

Autocorrelator can perform synchronization for frame ,time and frequency. It has been also proved that Autocorrelation is suitable for synchronization. After a careful analysis of competing algorithms, it is decided that the best choice for time synchronization is to use the basic Auto-Correlation estimator. To get more accuracy for estimating the frequency offsets, CORDIC algorithm is used**.** It is used for estimating the carrier frequency offsets as well as compensating those frequencies by estimating the phase of the maximum correlating signal. It is more advantageous to greatly reduces the delay while using the multiplier hardware. In previous methods for estimating the offsets, eventhough it achieves better result it lack accuracy. But in the proposed model, the given sample is serially iterated in order to achieve the bit of accuracy. It also achieves minimum resource utilization.The proposed model also proved that the utility of devices is lesser than the other existing model. In the end, the proposed design consumed an relatively low quantity of hardware resources, gives less delay and produced excellent results for packet detection, frequency offset estimation, and time, frequency synchronization.

VII. FUTURE WORK

By getting the better results, it is also decided that the quantized 64 sample cross correlator, in conjunction with the maximum detector, it would be used for fine time synchronization. On analysis, it is obtained that the fast pipelined CORDIC architecture drastically increases area and power by increasing number of iterations and number of cells usage. Thus the algorithm is greatly enhanced in future use. This design can also be implemented in FPGA or ASIC to achieve the spectral efficiency in OFDM WLAN reciever. The minimization of the power difference or maximizing the SINR approaches could be considered to optimize the compensation process such that the system performance is improved. From the architectural point of view where the iterative process adds more challenge to the design of the synchronization unit. Furthermore, the timing and frequency synchronization architecture unit could be evaluated in a testbed OFDM system.

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