Design and Simulation of High Performance Low Power Control Circuits at Gate and Layout Levels

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Abstract:

Many integrated circuits of today contain a very large number of transistors, over 1 million in some designs. The aim is to design a low power high performance sequencer and program counter, analyze and simulate at gate and layout levels. High level description language to be used to construct layout of program counter and sequencer.

Keywords: Sequencer, Controller, Program Counter, Low Leakage.

I. Introduction:

The program counter plays a very important role in the design of microprocessor as it supplies the main program memory with the address of the active instruction. The program counter is like someone pointing a finger at the list of instructions, saying do this first, do this second, ad so on. This is the reason program counter is sometimes called pointer*;* it points to an address in memory where something important is being stored. The sequencer is the heart of the microprocessor, it controls the most important signals generated in the microprocessor.

II. Circuit Implementation of Low Power High Performance Program Counter and Sequencer

The program is stored at the beginning of the memory with the first instruction at binary address 0000, the second instruction at address 0001, the third at address 0010 and so on. The program counter, which is part of the control unit, counts from 0000 to 1111.

Its job is to send to the memory the address of the next instruction to be fetched and executed. At start, the program counter is 0. Then, at the end of each instruction, the program counter is incremented, in order to select the next instruction [2].

One simple way to build this counter is to chain edge sensitive D-registers as shown in Figure 1. This circuit works asynchronously. The PC is reset to 0000 before each computer run. When the computer run begins, the program counter sends the address 0000 to the memory. The program counter is then incremented to 0001. After the first instruction is fetched and executed, the program counter sends the next address 0001 to the memory. Again the program counter is incremented. After the second instruction is fetched and executed, the program counter sends address 0010 to the memory. In this way, the program counter is keeping track of next instruction to be fetched and executed. In this work Program Counter is designed for 4 bit and a maximum of 16 instructions can be addressed. This is designed using 4 D-flip flops in asynchronous type. Figure 1 depicts its design.

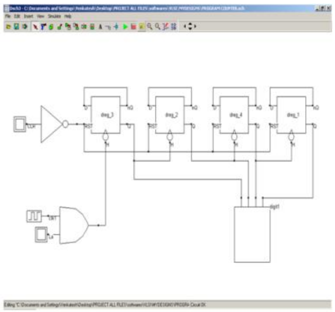


Figure 1 Schematic view of Program counter.

The sequencer is the main part of the microprocessor. It controls the most important signals such as the enable and latch controls. The input to the sequencer is the instruction code itself, as well as the phase information. The four input AND gates serve as instruction decoders. Depending on the type of instruction, the desired signals are set to 1 if active, or kept at 0 to be inactive. The schematic view of the sequencer is as shown in Figure 2.

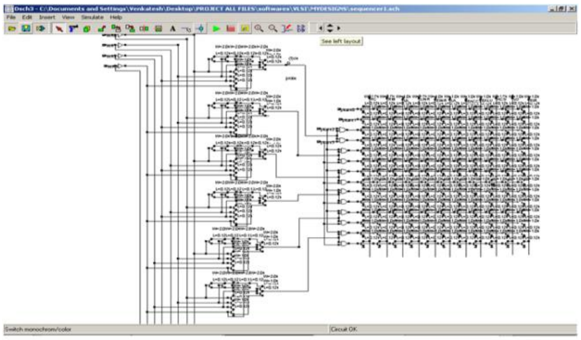


Figure 2 Schematic view of the sequencer.

III. Analysis of Leakage Power Consumption of Program Counter and Sequencer

The leakage current is the current that flows between Drain and Source when no channel is present [2]. No current is expected to flow between drain and source. However, a leakage current enables nA range current to flow although the gate voltage is 0. Considering the program counter and sequencer, the schematic diagram of the counter is shown in Figure 1 and its layout implementation in Figure 3 and the schematic of sequencer in Figure 2 and its layout in Figure 4. Here, we analyze its switching performances, in the high speed and low leakage modes.

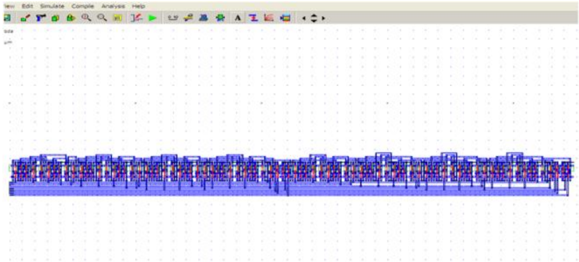


Figure 3 Layout of Program Counter

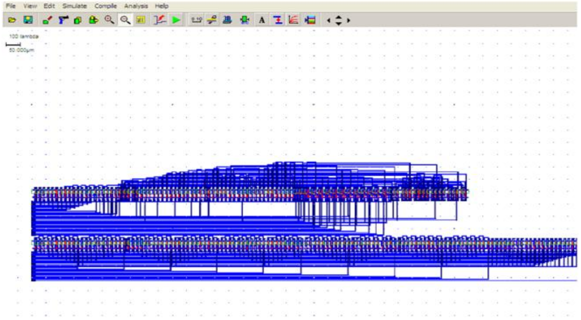


Figure 4 Layout of Sequencer.

In the high speed mode, the circuits works fast (900 MHz) but consumes a significant standby current when off (around 200 nA). This is as shown in Figure 5.

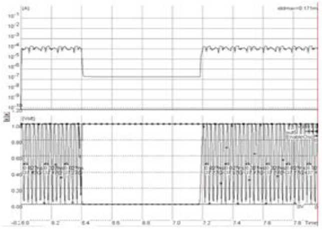


Figure 5 High Speed Mode

Once tne option layer is set to “low leakage”, the simulation is performed again. The low- leakage mode features a little slower (100Mz that is approximately a 9 % speed reduction) and more than one decade less standby current when off (5 nA). In summary, low leakage MOS devices should be used as default devices whenever possible. High speed MOS should be used only when switching speed is critical. This is shown in Figure 6.

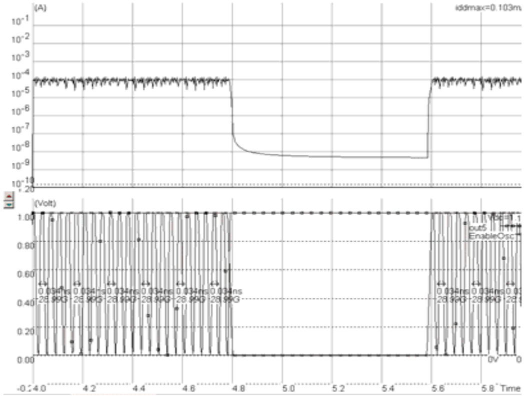
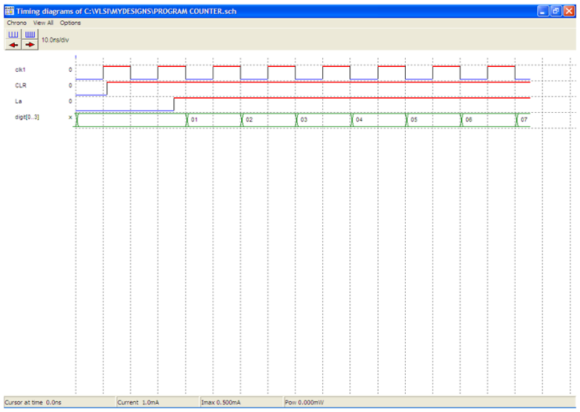


Figure 6 Low Leakage Mode.

IV. Result and Discussion of Program Counter and Sequencer:

The simulation result of the program counter is performed by enabling the clear input and applying the clock signal. The number of transistors used for designing the program counter is 54. From Figure 7 we can see that the maximum current (Imax) consumed by this program counter is approximately 0.5mA and the power dissipated by this circuit is 0mW.

From Figure 7 it is evident that when the clear signal is set high and the flip-flops are enabled, the program counter starts counting from 0 to 15.



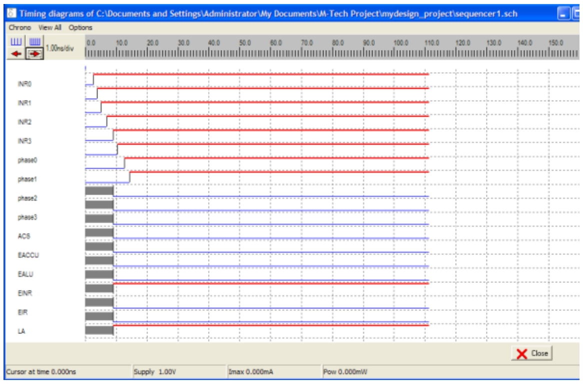
Timing diagrams of C:\VLSI\MYDESIGNS\PROGRAM COUNTER.sch

Cursor at time 0.0ns | Current 1.0mA | Imax 0.500mA | Pow 0.000mW

Figure 7 Simulation result of Program Counter.

The simulation result of the sequencer is as shown in Figure 8. The different control signals that this sequencer generates are displayed in Figure 8. From the figure we can see that the control signals that are set high are RM and LINR. Hence, when these signals are activated, the corresponding operation performed by the microprocessor is, the contents from the memory are latched on to the instruction register.

The number of transistors used for designing the controller is 294. The maximum current (Imax) consumed by the sequencer during its operation is approximately 0.0mA and the power dissipated by this controller is 0mW.

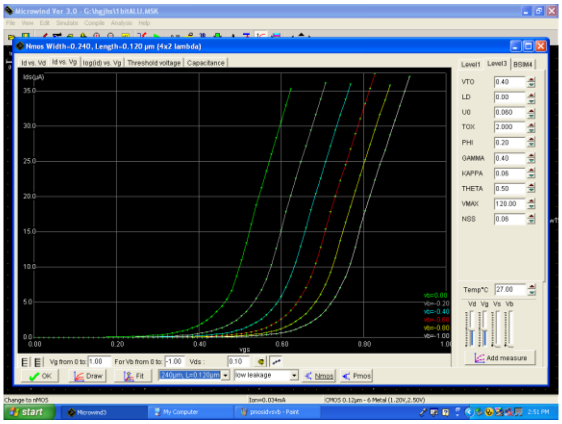


Timing diagrams of C:\Documents and Settings\Administrator\My Documents\M-Tech Project\mydesign_project\sequencer1.sch

Cursor at time 0.000ns | Supply 1.00V | Imax 0.000mA | Pow 0.000mW

Figure 8 Simulation result of Sequencer.

The main objective of the low leakage MOS is to reduce the *Ioff* current significantly, that is the small current that flows between drain and source with a zero gate voltage. The price to pay is a reduced *Ion* current. The designer has the possibility to use high speed MOS devices, which have high *Ioff* leakages but large *Ion* drive currents. The size correspond to the 0.12µm technology [3]. In Figure 9 and Figure 10, the characteristics of NMOS and PMOS is plotted. Both the low leakage MOS device has an negligible *Ioff* current. Thanks to a higher threshold voltage (0.4V rather than 0.3V) and larger effective channel length (120nm) compared to the high speed MOS. In the work, low leakage transistors are selected to encourage low power design. The *Ion* difference is around 33%. This means that a high speed MOS device is 33% faster than the low leakage MOS.



Microwind Ver 3.0 - G:\hgjhs\1bitALU.MSK

Nmos Width=0.240, Length=0.120 µm (4x2 lambda)

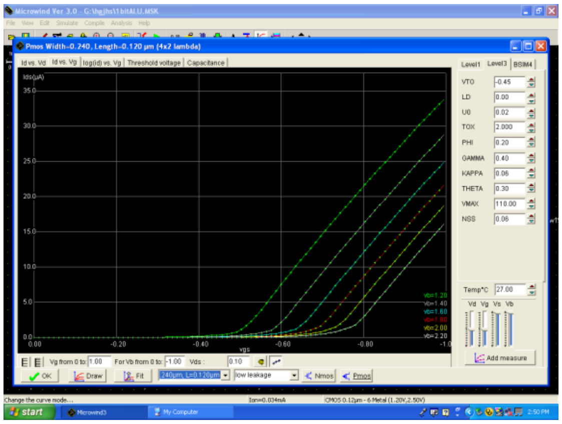
VTO 0.40
LD 0.00
U0 0.060
TOX 2.000
PHI 0.20
GAMMA 0.40
KAPPA 0.06
THETA 0.50
VMAX 120.00
NSS 0.06
Temp°C 27.00

Vg from 0 to: 1.00 | For Vb from 0 to: -1.00 | Vds : 0.10 | 240µm, L=0.120µm | low leakage

Change to nMOS | Ion=0.034mA | CMOS 0.12µm - 6 Metal (1.20V,2.50V)

Figure 9 NMOS Device Characteristics

Therefore, from the above analysis and results we can draw conclusion that a proper selection of transistors and designs move toward lower V_{DD} and lower V_{TH} reducing power dissipation. In this way it is evident from the above discussion that optimizing V_{DD} and V_{TH} is essential in low power, high speed designs.



Microwind Ver 3.0 - G:\hgjhs\1bitALU.MSK

Pmos Width=0.240, Length=0.120 µm (4x2 lambda)

VTO -0.45
LD 0.00
U0 0.02
TOX 2.000
PHI 0.20
GAMMA 0.40
KAPPA 0.06
THETA 0.30
VMAX 110.00
NSS 0.06
Temp°C 27.00

Vg from 0 to: 1.00 | For Vb from 0 to: -1.00 | Vds : 0.10 | 240µm, L=0.120µm | low leakage

Change the curve mode... | Ion=0.034mA | CMOS 0.12µm - 6 Metal (1.20V,2.50V)

Figure 10 PMOS Device Characteristics

V. Conclusion and Scope for Future Work

Design, analysis and simulation of a Program Counter and Sequencer at gate and layout levels is presented. Both these circuits are designed for high performance and low power. The circuits are tested and simulated at transistor; gate and layout levels. The circuit is also tested by varying the threshold voltage. These circuits operates at a frequency range of 100MHz to 900MHz with a wide operating voltage of 1.2V to 5V. The technology employed is 120nm.

Leakage current can be reduced by adaptive body biasing and embedding dual threshold voltage in the proposed architecture. Power can be reduced by employing a technique of controlling threshold voltage through substrate bias.

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