Power Management in At- Speed Scan Based Testing Applied to SOC

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Abstract:
The focal goal of this paper is to shrink power consumption for the duration of at speed scan based testing. In scan-based tests, power consumptions in both shift and capture phase may be drastically privileged than that in regular approach, which threaten circuits' trustworthiness through manufacturing test. High power consumed during shift and capture phases upshot in structural smash up to silicon or flawed data transmit during manufacturing test. Prior X filling techniques diminish either shift power or capture power however not together. Work of fiction Proposed X filling technique that can dwindle both shift- and capture-power for the period of speed scan based testing. Further still more reduce power consumption by adding dynamic voltage scaling method with X-filling method.

Keywords---At-Speed Scan-Based Testing, Low-Power Testing, Dynamic voltage scaling, X-Filling Technique

I. INTRODUCTION

With the advent of deep sub-micron technology and tight yield and reliability constraints, in order to perform a non-destructive test for high performance VLSI circuits power dissipation during test application should not exceed the power constraint set by the power dissipated during functional operation of the circuit. This is because excessive power dissipation during test application caused by high switching activity may lead to the following two problems namely
Destructive testing& Manufacturing yield loss

The power dissipation of integrated circuits (ICs) in scan-based testing can be significantly higher than that during normal operation [1]. This will threaten the reliability of the circuits under test (CUT), because: (i) the elevated average power dissipation adds to the thermal load that must be transported away from the CUT and can cause structural damage to the silicon, bonding wires, or the package; (ii) the excessive peak power dissipation is likely to cause a large voltage drop that may lead to erroneous data transfer in test mode only, especially in at-speed testing, thus invalidating the testing process and leading to yield loss.

In this effort, we focus on one of the most widely-used software-based solutions for test power reduction, which tries to reduce the CUT's switching activities by filling the don't-care bits (i.e., *X-bits*) in given test cubes intelligently, known as the *X-filling* technique.

In the this approach X-filling technique, first, we try to fill as few as possible X-bits to keep the capture-power under the peak power limit of the CUT to avoid test overkills, and then use the remaining X-bits to reduce shift-power as much as possible to cut down the CUT's average power consumption. Moreover, the X-filling technique is able to reduce power consumptions in both shift-in and shift-out processes, thus leading to significant shift-power reduction.

Dynamic voltage scaling is a power management technique in computer architecture, where the voltage used in a component is increased or decreased, depending upon circumstances. Dynamic voltage scaling to increase voltage is known as **overvolting**; dynamic voltage scaling to decrease voltage is known as **undervolting**. Undervolting is done in order to conserve power, particularly in laptops and other mobile devices, where energy comes from a battery and thus is limited. Overvolting is done in order to increase computer performance, or in rare cases, to increase reliability.

By Dynamic Voltage Scaling technique with X-filling, further we reduce power consumption in CUT's.

II. BACKGROUND

A. *Power Consumption in At-Speed Scan-Based Testing*

At-speed scan-based tests facilitate to detect speed-related defects of the CUTs and have been widely utilized in the industry in recent years, which typically involve a long low-frequency shift phase and a short at-speed capture phase. There are mainly two types of at-speed scan-based testing approaches: Launch-on-Shift (LoS) and Launch-on-Capture (LoC). LoC scheme is more widely utilized because it does not need the expensive high-speed scan-enable signal required by the LoS scheme. As shown in Fig. 1, there are three types of clock signals in LoC scheme: "SCLK" represents the shift clock signal, under which the test vectors are shift-in/out of the scan chains; "ACLK" is the at-speed clock in the CUT to be

applied in the capture phase; "TCLK" is the clock signal that the sequential elements on the scan chain will receive, by MUXing "SCLK" and "ACLK" signals. Typically two capture cycles (C1 and C2) are used to detect defects. We denote the initial state of the scan cells and the nodes in combinational portion of the circuit before capture as S1. The first capture C1 launches the state S2 into the CUT, while the second capture C2 store the circuit state S3 after the CUT is applied in functional mode.

The data input *DI* of each scan cell is connected to the output of the combinational logic as in the original circuit. To form a scan chain, the scan inputs *SI* of SFF_2 and SFF_3 are connected to the outputs Q of the previous scan cells, SFF_1 and SFF_2, respectively. In addition, the scan input *SI* of the first scan cell SFF_1 is connected to the primary input *SI*, and the output Q of the last scan cell SFF_3 is connected to the primary output *SO*. Hence, in shift mode, *SE* is set to 1, and the scan cells operate as a single scan chain, which allows us to shift in any combination of logic values into the scan cells. In capture mode, *SE* is set to 0, and the scan cells are used to capture the test response from the combinational logic when a clock is applied

Timing diagram to illustrate how the full-scan design is utilized to test the circuit shown in Figure 2.14a for stuck-at faults. During test, the test mode signal *TM* is set to 1, in order to turn on all test-related fixes.Two test vectors, V1 and V2, are applied to the circuit. In order to apply V1, *SE* is first set to 1 to operate the circuit in shift mode, and three clock pulses are applied to the clock *CK*. As a result, the PPI portion of V1, denoted by V_1:PPI, is now applied to the combinational logic. A **hold cycle** is introduced between the shift and capture operations. During the holdcycle, *SE* is switched to 0 such that the muxed-D scan cells are operated in capturemode, and the PI portion of *V*1, denoted by *V*1:PI, is applied. The purpose of thehold cycle is to apply the PI portion of *V*1 and to give enough time for the globally routed *SE* signal to settle from 1 to 0. At the end of the hold cycle, the complete test vector is now applied to the combinational logic, and the logic values at the primary outputs PO are compared with their expected values. Next, the capture operation is conducted by applying one clock pulse to the clock *CK* in order to capture the test response of the combinational logic to V1 into the scan cells. A second hold cycle is added in order to switch *SE* back to 1 and to observe the PPO value of the last scan cell at the *SO* output. Next, a new shift operation is conducted to shift out the test response captured in the scan cells serially through *SO*, while shifting in V2:PPI, which is the PPI portion of the next test pattern V_2.

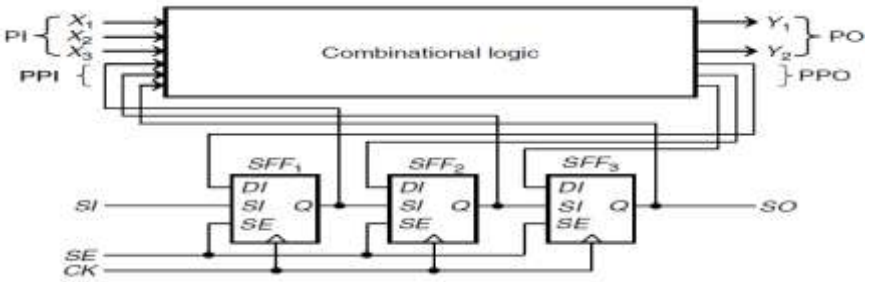

Fig-1: Example Circuit

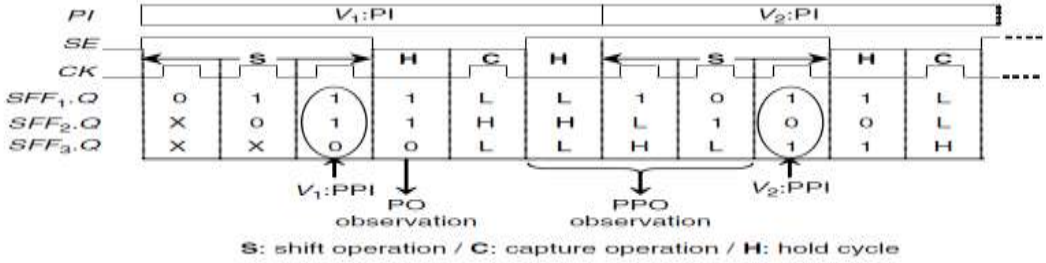

Fig-2: Timing Diagram for At-Speed Test operation

The shift process in scan-based testing not only dominates the test time of the CUT, but also determines the CUT's accumulated power dissipation. The main objective in shift-power reduction is thus to decrease it *as much as possible*, so that higher shift frequency and/or increase test parallelism can be applied to reduce the CUT's test time and hence cut down the test cost, under the average power constraint of the CUT.

In capture mode, on the other hand, since the duration is very short, it has limited impact on the CUT's accumulated test power consumption. However, because test vectors are usually generated to detect as many faults as possible, the excessive Transitions in capture phase may cause serious IR-drop and prolong circuit delay, thus causing false rejects (i.e., good chips fail the test) in at-speed tests. Consequently, the main objective in capture- power reduction is to keep it under a safe threshold to avoid test overkill. As long as this requirement is fulfilled, there is *no* need to further reduce capture-power.

B. Dynamic voltage scaling

MOSFET-based digital circuits operate using voltages at circuit nodes to represent logical state. The voltage at these nodes switches between a high voltage and a low voltage during normal operation—when the inputs to a logic gate transition, the transistors making up that gate may toggle the gate's output.

At each node in a circuit is a certain amount of capacitance. Capacitance can be thought of as a measure of how long it takes for a given current to effect a given voltage change. The node; since currents are related to voltage, the time it takes depends on the voltage applied. By applying a higher voltage to the devices in a circuit, the capacitances are charged and discharged more quickly, resulting in faster operation of the circuit and allowing for higher frequency operation. In this block diagram there are three main components. The first component is a performance sensor that monitors the main capacitance arises from various sources, mainly transistors (primarily gate capacitance and diffusion capacitance) and wires (coupling capacitance).

Here, we present a closed loop configuration based on fuzzy logic (FL) controllers to adaptively adjust the supply voltage of the processor compatible with workload variations. FL controllers are well suited for low-cost implementations based on cheap sensors and low-resolution analog-to-digital converters. Such systems can be easily upgraded by adding new rules to improve performance or add new features. Furthermore, in closed loop adaptive voltage scaling most of the power is dissipated in the time interval between changing the workload and acting to change the supply voltage. Consequently predicting the processor's workload compensates this drawback. Also, FL controller can be used to enhance power savings in comparison to other traditional controller systems, especially when the rate of workload variations is high.

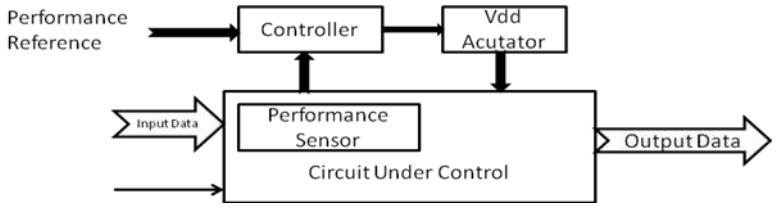

Fig 2: Block Diagram of Dynamic Voltage Scaling

C. Overview of Prior Work on Low-Power Testing

Adjacent fill is a simple yet effective technique targeting shift-power reduction. However, it can reduce the shift-in power only. We first addressed the low capture-power solution with X-filling. They considered the transitions at the output of SFFs during X-filling, which, however, does not necessarily have a good correlation with the total capture power of the whole circuit. Later, they took the above into consideration and introduced a new method to select the X-filling target based on a so-called set-simulation technique, which is proved to be a more effective X-filling method with experimental results on ISCAS'89 circuits. One of the main limitations of is that their computational time is quite high. This is because: (i). they are incremental filling approaches, that is, they fill the X-bits in the test cube one by one; (ii). Forward implications and backward justification are extensively used in their methodologies. In fact, the complexity of the set-simulation techniques proposed is quite high and it is difficult, if not impossible, to be applicable for two-pattern tests in industrial designs.

In developed an efficient probability-based X-filling technique, called *preferred fill*, which tries to fill all X-bits in the test cube in one step, instead of using incremental fill and logic simulation. Their technique, however, is inherently less effective as the available information for the probability calculation in their single-step filling is quite limited. Also, only transitions at the SFFs are considered while the transitions at logic gates are ignored in their work.

III. IMPACT ANALYSIS FOR X-FILLING

The impact of different X-bits on the CUT's shift- and capture-power (namely *S-impact* and *C-impact*, respectively).

A. Impact of X-Bits on Shift and Capture-Power

Test cube generally contains multiple X-bits, and as many-bits in the test response are likely to become determined values after filling one single X-bit in the test stimulus**,** their filling order significantly affects the CUT's test power dissipation. We therefore try to model the impact of an X-bit on a CUT's shift- and capture-power (namely *S-impact* and *C-impact*), and use them to guide the X-filling.

During the scan shift phase, the test stimuli are shifted in scan cells with previous test responses shifted out concurrently. To model the impact of an X-bit in the test stimuli on shift-power dissipation, we need to define a completely different cost factor because shift-power mainly concerns transitions between adjacent scan cells instead of switching activities in the entire CUT. Therefore, we first identify the scan cells in *S3* that are possibly affected by filling an X-bit in *S1* (denoted as S3i *affected S*), by tracing its fan-out logic network.

IV. PROPOSED X-FILLING TECHNIQUE

In this section, we detail our proposed *iFill* X-filling solution, including *C-filling* for capture-power reduction, *S-filling* for shift-power reduction, and the overall algorithm to achieve both shift- and capture-power reduction objectives. In addition, we show how to improve the runtime efficiency of the proposed solution.

B. C-Filling for Capture-Power Reduction

It is not necessary to reduce capture power as much as possible. Instead, we only need to control it to be smaller than a safe threshold and we wish to use as few as possible X-bits to achieve this objective, so that the remaining X-bits can be filled for shift-power reduction. Therefore, we need to fill X-bits with higher C-impact earlier.

The transition probability for a logic node in the capture cycle when filling X*i* is calculated as follows:

$$\mathbf{TP}i = \mathbf{P_{1i}}' \times \mathbf{P_{0i}} + \mathbf{P_{0i}} \times \mathbf{P_{1i}}'$$

Where P'1i(P'0i) is its probability to be "1" ("0") in S1, and P1i(P0i) is its probability to be "1" ("0") in S2.

The *Capture Transition Probability* (*CTP*) of the CUT caused by filling an X-bit X*i* in test stimuli can be calculated as sum of transition probabilities of X-bits in its fan-out part

$$CTPi = \sum_{j \in fan-out\ xi} TP\ j$$

Then we can decide the logic value to be filled for the target X-bit, which will cause less in fan-out portion of this scan cell.

C. S-Filling for Shift-Power Reduction

Prior work on X-filling for shift-power reduction considers shift-in power only. This is unfortunate, because filling these unspecified bits has impact on both shift-in and shift-out power consumption.

To model the shift transition probability caused by logic differences between X*i* and its adjacent scan cells in the test stimuli, we calculate the *shift-in transition probability* (*SITP*) caused by filling this X-bit as follows:

$$\text{S-impact}_i = \text{pi} + \sum_{j\text{es affected}} (l\ scj - P\ j$$

where P1s(P0s) represents the probability of X*i* to be 1 (0),*i* is the position this X-bit resides, which relates to transition number it may cause during the shift-in.

Where j ranges among all the X-bits affected by X*i*, and P1r (P0r) represents the probability of the response X-bit X*j* to be "1" ("0"). It should be noted that these X-bits in test responses can be in different scan chains.

Now we can determine the total *shift transition probability* (*STP*) when filling with "1" and "0", respectively. It can be simply calculated as the sum of its SITP and SOTP.

To reduce shift-power, we should fill X*i* with the logic value that will cause fewer transitions in both shift-in and shift-out phases. As shown in Fig. 4, if STPi(1)<STPi(0) , it means filling X*i* with logic "1" is likely to generate less circuit transitions during the scan shift phase than that of filling it with logic "0", so we should fill X*i* with logic "1". Otherwise, we should fill with logic "0".

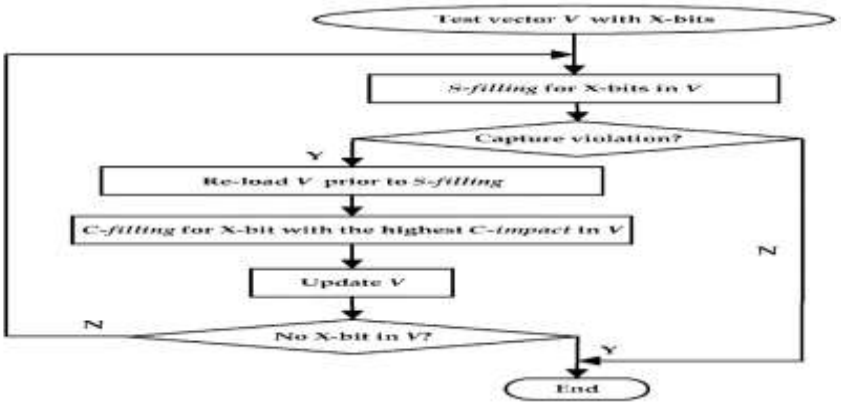

Fig-3 : S-Filling & C-Filling Flow for Power Reduction

D. Overall Flow

The objective of the proposed *X*-filling technique for simultaneous shift- and capture-power reduction is to keep the capture transitions under threshold and reduce shift transitions as much as possible. To meet this target, we proposed the overall flow as outlined in Fig. 4. First, we try to conduct *S-filling* to use all the X-bits in test vectors for shift-power reduction and check whether the capture-power violates the constraint after the *S-filling* process. If it does, we need to re-load the initial test cube, and fill one X-bit with the highest *C – impact* value for capture-power reduction. After filling every X-bit for capture- power reduction, the test vector will be updated, and we will apply *S-filling* procedure one more time to fill the remaining X-bits and then the capture-power will be checked again to see whether this test vector still has capture-power violation. When there is no power violation, we have completed filling the vector; Otherwise, *C-filling* procedure will be called again to reduce capture transitions. The above steps iterate themselves until there is no peak power violation or all X-bits have been utilized to reduce Capture-power. If the capture transitions still violates the limit after all X-bits have been filled, this test pattern need to be discard. After X-filling for all the test patterns in give test set, new test patterns need to be generated for the faults the test pattern violating the capture power limit covered.

E. DYNAMIC VOLTAGE SCALING

The *switching power* dissipated by a chip using static CMOS gates is $C \cdot V^2 \cdot f$, where C is the capacitance being switched per clock cycle, V is voltage, and f is the switching frequency,[1] so this part of the power consumption decreases quadratically with voltage. The formula is not exact however, as many modern chips are not implemented using 100% CMOS, but also uses pseudo nMOS gates, domino logic etc. Moreover, there is also a static leakage current, which has become more and more accentuated as feature sizes have become smaller (below 90 nanometres) and threshold levels lower.

Accordingly, dynamic voltage scaling is widely used as part of strategies to manage switching power consumption in battery powered devices such as cell phones and laptop computers. Low voltage modes are used in conjunction with lowered clock frequencies to minimize power consumption associated with components such as CPUs and DSPs; only when significant computational power is needed will the voltage and frequency be raised.

Some peripherals also support low voltage operational modes. When leakage current is a significant factor in terms of power consumption, chips are often designed so that portions of them can be powered completely off. This is not usually viewed as being dynamic voltage scaling, because it is not transparent to software.

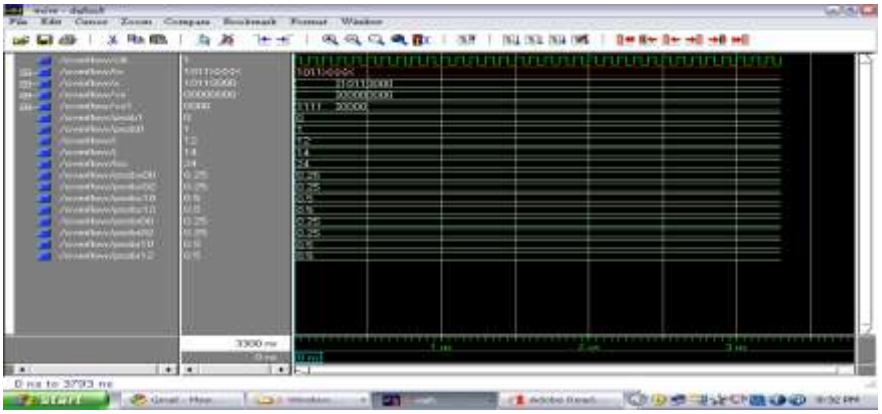

Fig-4:.Simulation Result for Overall

V. CONCLUSIONS

This paper presents an effective and efficient impact-oriented X-filling method, which is able to keep the CUT's capture-power within its peak power rating while reduce the CUT's shift-power as much as possible. Another contribution of the proposed technique is that it is able to cut down power consumptions in both shift-in and shift-out processes. In this work, all X-bits in given test cubes are used for test power reduction. Hardware implementation of Dynamic Voltage Scaling method with X-filling, we can reduce Power consumption of Entire CUT's.

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