Image compression Algorithm Implementation on Reconfigurable platform

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Abstract - This paper presents an approach towards FPGA implementation for image compression. The design follows the JPEG2000 standard and can be used for both lossy and lossless compression. The embedded block coding with optimized truncation (EBCOT) is a key algorithm in JPEG 2000 image compression system. Various applications, such as medical imaging, satellite imagery, digital cinema, and others, require high speed, high performance EBCOT architecture. Though efficient EBCOT architectures have been proposed, hardware requirement of these existing architectures is very high and throughput is low. To solve this problem, the performance of the coder is improved and the entire design of EBCOT encoder is tested on the field programmable gate array platform.

Index Terms - image compression, discrete wavelet transforms (DWT), JPEG 2000, and FPGA.

I. INDRODUCTION

With the use of more and more digital still and moving images, huge amount of disk space is required for storage And manipulation purpose. For example, a standard 35-mm photograph digitized at 12µm per pixel requires about 18Mbytes of storage

And one second of NTSC-quality color video requires 23 Mbytes of storage. That is why image compression is very important in order to reduce the storage need. Digital images can be compressed by eliminating redundant information present in the image, such as spatial redundancy, spectral redundancy and temporal redundancy. The removal of spatial and spectral redundancy is often accomplished by transform coding. Which uses some reversible linear transform to decor relate the image data.JPEG is the most commonly used image compression standard in today's world. But researchers have found that JPEG has many limitations. In order to overcome all those limitations and to add on new improved features, researchers has come up with new image compression standard, which is JPEG2000.The JPEG2000 is intended to provide a new image Coding/decoding system using state of the art compression techniques, based on the use of wavelet technology. Its wide range of usage includes from portable digital cameras through pre-press, medical imaging. Right now, JPEG2000 is composed of 6 main parts. The two important parts in the coding/decoding processes of JPEG2000 are Wavelet Transform and Arithmetic Coding. Since the later is widely implemented, this paper focuses on the hardware implementation of discrete wavelet transform and EBCOT Algorithm. The Fig.1 shows the basic building blocks of JPEG2000 encoding process.

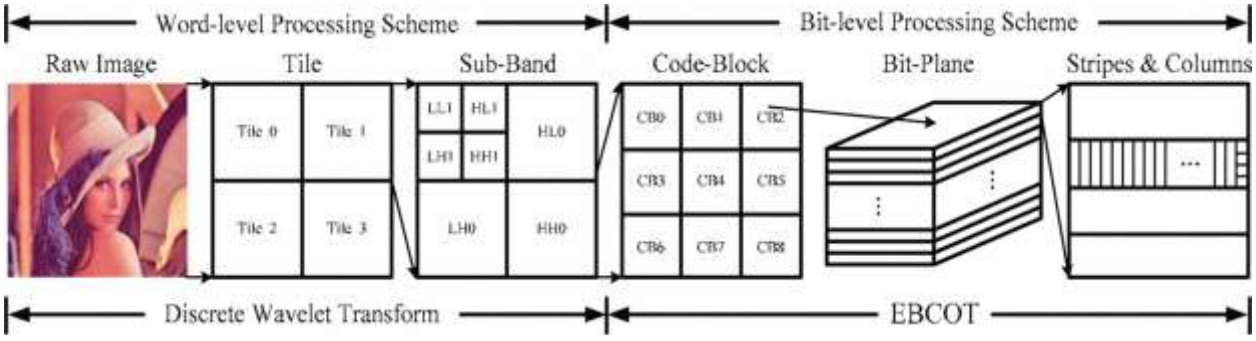

Fig.1.a) Basic building blocks of JPEG 2000

II. LIFTING SCHEME FOR WAVELET TRANSFORM

Lifting scheme is new method on spatial to construct wavelets which consist of three steps: split, predict and update. Lifting wavelet is called the second generation wavelet. The basic principle of which is to break up the polyphase matrices for wavelet filters into sequence of upper and lower triangular matrices and convert the filter implementation into banded matrix multiplications. The DWT lifting scheme is shown in figure.

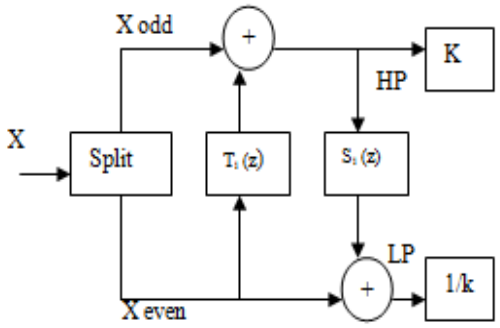

Fig 1.b) Lifting Scheme

The JPEG2000 adopts the discrete wavelet transform as its primary transforming algorithm. The overall block diagram of JPEG2000 is shown in Fig. 1. The transformed coefficients are split into code blocks and are sequentially processed by an entropy coding algorithm known as embedded block coding with optimized truncation (EBCOT). The EBCOT is the most complicated part that accounts for the majority of the computation time in the JPEG2000 encoding system. [3]

This is due to the fact that EBCOT is inherently a bit-level operation which cannot be executed efficiently in software. As shown in Fig. 1, while the DWT is a word-level processing scheme, EBCOT is inherently a bit-level processing algorithm, causing the computational complexity in JPEG2000. Therefore, developing a high performance EBCOT unit is crucial in developing an efficient JPEG2000 application system.

III. OVERVIEW OF EBCOT ALGORITHM

The EBCOT is basically a two-tiered algorithm consisting of Tier-1 and Tier-2 called the embedded block coding and the rate distortion optimization, respectively. Tier-1 is again divided into two sub-modules: bit-plane coder (BPC) and binary arithmetic coder (BAC). The BPC utilizes the neighboring information of the current bit to construct the context information consisting of *context* (CX) and *decision* (D), which will be entropy coded by the following BAC. The major timing limitation is caused by the BAC, because it is inherently dependent on control statements and arithmetic operations. As a result, the BAC becomes a throughput bottleneck of the entire JPEG2000 encoding system, but its serial processing nature makes it difficult to exploit parallelism. Several pipelining techniques have been proposed in previous researches, but the processing speed of the BPCs suggested so far still exceeds that of current BAC architectures. Therefore, improving the BAC Throughput would potentially increase the overall performance of JPEG2000 systems.

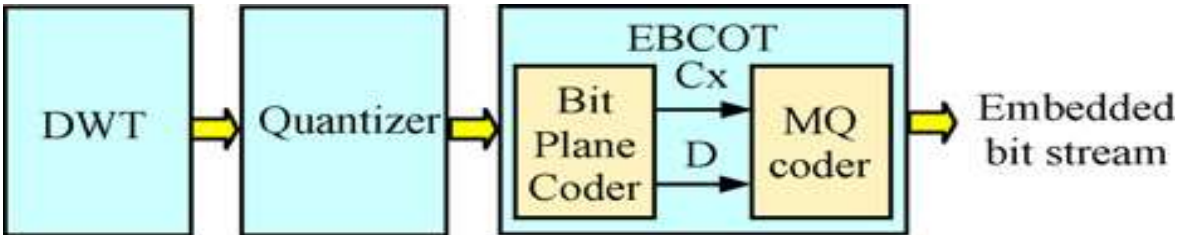

Fig. 2.Over view of EBCOT

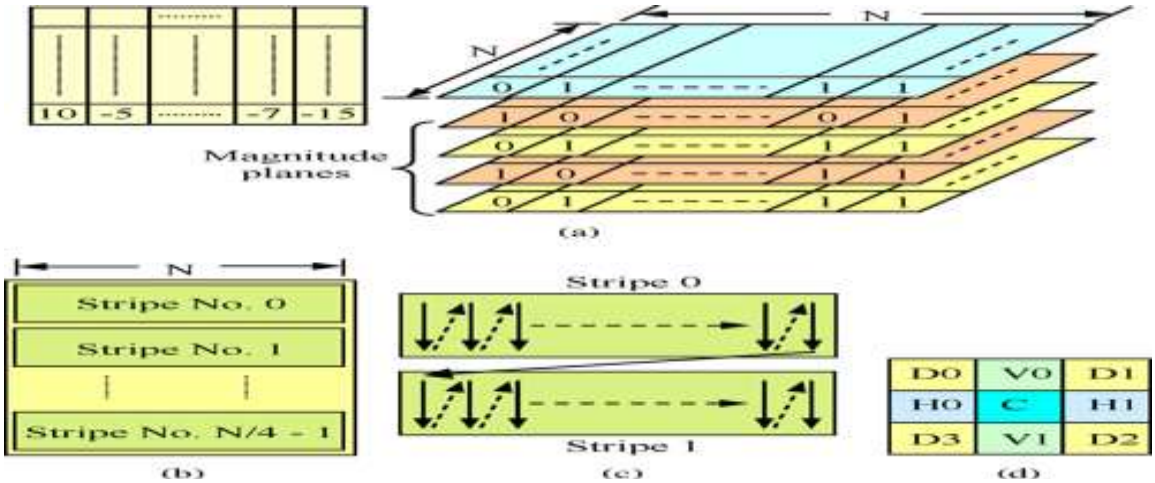

Fig.3.Samples scanning order in BPC

In Tier-1, Wavelet sub-bands are partitioned in to small code blocks which in turn are coded by bit planes. The bit – plane structure is illustrated in fig 3.The most significant bits are coded first, and then lower-order bits are coded in descending order. Each bit plane is coded separately as if it was a bi-level image. Each bit plane is coded in three passes (i) significant propagation pass (ii) magnitude refinement pass (iii) clean-up pass. During significant propagation pass, a bit is coded if its location is not significant, but at least one of its eight-connected neighbors is significant. All the bits that have not been coded in significant propagation pass and became significant in a previous biplane are coded in the pass. In clean–up pass all the bits that have not been coded in either significant propagation pass or magnitude refinement pass are coded in this pass. The clean-up pass also performs a form of run-length coding to efficiently code a string of zeros.

In each pass, only a part of the bit plane is coded and each bit position is coded only once by one of the three passes each coding pass constitutes an atomic code unit, called chunk code-word chunks are grouped into quality layers and can be transmitted in any order, provided the chunks that belongs to the same code block are transmitted in their relative order .chunks constitute valid truncation points. Both the encoder and the decoder can truncate the bit stream in correspondence of a valid truncation point in order to recover the original data up to a target quality.

IV.FPGAs

Traditionally computations requiring the high performance of a custom hardware implementation Involved the development and fabrication of an Application Specific Integrated Circuit (ASIC). Development of an ASIC requires several steps. The circuits must be designed and then fabricated. Fabrication involves creating wafer masks for that specific design, fabricating the chips, packaging and finally testing. A modification to a design postmasking requires whole new wafer masks to be prepared. All of these factors contribute to making ASIC designs both expensive for low volume runs and intolerant to design errors or modifications once the fabrication process is started. With the advent of Field Programmable Gate Arrays (FPGAs) and Reconfigurable Computing, designers may now develop custom hardware solutions without a separate fabrication run for each design. FPGAs are, as their name implies, an array of logic gates, which can be programmed to perform a variety of tasks. They consist of programmable logic structures distributed throughout the chip. A routing interconnect is used to connect the logic structures. Like the array of logic gates, the routing interconnect is fully programmable. By reprogramming the logic gates and the routing interconnect it is possible to configure the chip to perform any arbitrary computation. Current devices can handle circuits with millions of gates, running at 50 MHz or more. Utilizing their programmable nature, FPGAs offer a low cost, flexible solution over traditional ASICs. Since a single FPGA design since a single FPGA design may be used for many tasks, it can be fabricated in higher volumes, lowering fabrication costs. Also, their ability to be reprogrammed allows for easy design modifications and bug fixes without the need to construct a new hardware system.

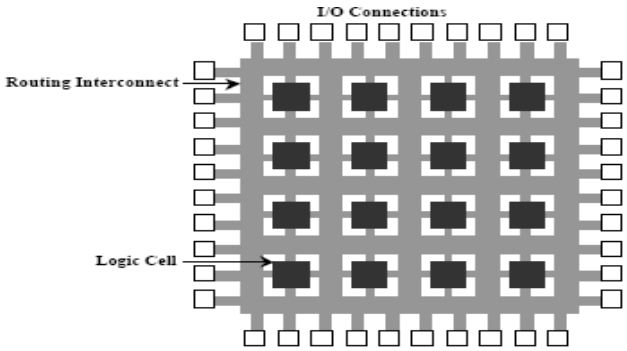

Fig.4.Typical FPGA Structure

IV. CONCLUSION

The architecture for the image compression has been proposed, which is based on JPEG 2000 standard. The proposed architecture can reduce the internal memory size, between the DWT and EBCOT stages. The number of accessing storage and will improve the throughput. This has been implemented and tested in MATLAB. After this, it can be implemented in FPGA for many image processing applications in Real time.

V. REFERENCES

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