Oscillation Test Methodology for Built-In Analog Circuits

Ms. Sankari.M.S and Mr.P.SathishKumar
Department of ECE, Amrita School of Engineering, Bangalore, India

Abstract
This article aims to describe the fundamentals of analog and digital testing methods to analyze the difficulties of analog testing and to develop an approach to test the analog components in a mixed signal circuit environment. Oscillation based, built-in self-test methodology for testing analog components in mixed-signal circuits, in particular, is discussed. A major advantage of the OBIST method is that it does not require any complex response analyzers and test vector generators which are costly Furthermore, since the oscillation frequency is considered to be digital it can be easily interfaced to test techniques dedicated to the digital part of the circuit under test (CUT). OBIST techniques show promise in detecting faults in mixed signal circuits and requires little modification of the CUT to improve the fault coverage. Extensive simulation results on some sample analog benchmark circuits are described in Spice format.

Keywords- System on chip (SOC), built-in Self test (BIST), Oscillation based built-in self test(OBIST), Circuit Under Test(CUT), Design for Testabiltity (DFT).

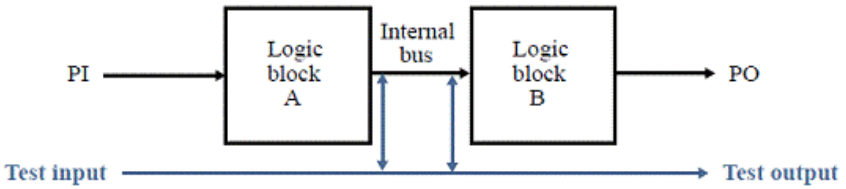
1. Introduction
Testing is a critical technology in the semiconductor production process. IC test is used for debugging, diagnosing and repairing the sub-assemblies in their new environment. The test should be designed to indicate the desired perfection. The objective is to realize through detailed testing, that the manufactured products are free from defects. It may ultimately help in increasing the product yield and reducing the product cost. The VLSI realization process has a distributed form of testing. Requirements and specifications are audited, design and tests are verified, and fabricated parts are tested. The broad specifications of analog circuits require detailed and long performance tests as well. This results in lengthy time consuming and very expensive test procedures. These factors have resulted in ample research being channeled in the direction of mixed signal testing. Researchers are now seeking to combine both analog and digital-circuits testing either by applying digital signals to drive analog circuits or by using analog signals to drive digital circuits. The applications of analog and mixed-signal, embedded-core-based, system-on-chip in recent years have motivated system designers and test engineers to direct their research to develop methodologies in effective very large-scale integrated circuits and systems testing. Mixed signal hardware systems have digital cores, very often interconnected with analog filters, analog and digital converters for digital processing. Testing is done to detect defects and diagnosis to determine the root cause of the defects. This would help in finding points in the process to be altered. If the product fails even after a detailed, rigorous and exhaustive test procedure, then pitfalls in the specification, design, or the fabrication process is suspected. The IC fabrication process involves photolithography, printing, etching, and doping steps. It is difficult to achieve 100% perfection in these steps while fabricating. Minor imperfections do creep in, leading to failures in the operation of the individual ICs. In the case of mixed signal ICs, the performance will not be satisfactory. The main sources of test difficulties in digital and analog circuits are also different. The size and complexity in digital circuits remain a measure of test difficulty whereas in analog and mixed-signal circuits, the behavior of circuit signals are much more important than circuit sizes. A major problem in the analog and mixed-signal-circuit testing is in defining the line of demarcation between a fault-free and faulty circuit, which leads to uncertainty in quantification of the product yield. In mixed signal circuits, imperfection in the form of small capacitance like parasitic, between the traces, produce a significant parameter variation altering the circuit behavior., Many parts of SOC are not accessible due to SOC complexity and limited test pins .To improve monitoring and control, test buses and scan chains are used by DFT methodology. Here, analog signals get degraded in long wire transmission resulting in erroneous test results and reduced production yield. One vital solution to this problem is by introducing Built-in self-test mechanism that permits a machine to test itself. The test generation, test application and response verification, all are accomplished through a Built-in hardware, which allows different parts of the chip to be tested in parallel. The test hardware can be placed near to the digital portion of the SOC which reduces the test time and eliminates the usage of external test t equipment. This concept originated with the idea of including pseudorandom number generator and cyclic redundancy check on the IC. BIST functionality is incorporated with the system level design. Fault models from the digital domain, like stuck-at faults, stuck on, stuck open, bridging faults, digital DFT and test techniques cannot be directly extended to analog circuits. Typically, analog circuits are tested by verifying against specifications. Test inputs can be generated easily for this straightforward method. Analog circuits have detailed, extensive specifications. Checking all the specifications is time consuming and expensive. Analog circuit signal monitoring is reduced in a mixed signal system. Since the testing of mixed signal circuit is complex, some effort is to be taken to lower the cost of test, particularly for the analog portions of mixed signal circuits. Almost every mixed-signal

integrated system contains circuits such as operational amplifiers, filters, oscillators, PLLs, etc. In this paper, an approach to develop a test methodology based on oscillation based built-in self-test is investigated. During the test mode, all these circuits (CUTs) could be transformed to an oscillator so as to make it testable by connecting some additional circuitry (a feedback network). In the process, the defined fault model and test algorithms considered to test the circuits in the mixed signal SOC environment and simulation results are provided for the selective benchmark circuits.

2. Test Methods

DESIGN FOR TESTABILITY (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity and test application cost. The basic concept of design for testability is given in Fig. 1. The test generation complexity increases exponentially with size of the chip.



.

Fig .1. Design for Testability

GENERAL BIST ENVIRONMENT

It is a design process that provides the capability of solving many of the problems encountered in testing analog, mixed-signal or digital systems. Test generation, test application and response verification is through Built-in hardware. It allows different parts of the chip tested in parallel thereby reducing the required testing time. It eliminates the necessity for external test equipment. BIST circuitry is located in the digital portion of the mixed-signal circuitry to minimize area overhead. The basic principle of BIST is explained in the Fig.2.

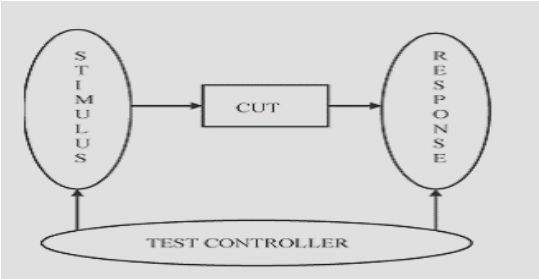


Fig .2 BIST Environments

A **built-in self-test (BIST)** or **built-in test** is a mechanism that permits a machine to test itself. Engineers design BISTs which ensure high reliability and reduced repair cycles. In integrated circuits, BIST is used to make faster, less-expensive manufacturing tests. The IC has a function that verifies all or a portion of the internal functionality of the IC. A BIST mechanism is provided in advanced field bus systems to verify its functionality. It reduces test-cycle duration.

3. Building of an Oscillator

The way to design a sinusoidal oscillator from the transfer function is to connect the output terminal of the filter to the input terminal. The basic requirements for oscillation are a signal feedback from the output to the input of proper phase and sufficient amplitude. The design equations of an oscillator are determined by analyzing the denominator of the transfer equation of the circuit. The poles of the denominator of the characteristic equation, or the zeros of $T(s)$, determine the time-domain behavior and stability of the system. The magnitude and phase equations of an oscillator must also be analyzed. If the magnitude of the loop-gain is greater than one and the phase is zero, the amplitude of oscillation will increase exponentially.

The process of building general oscillators is different than that of building oscillators for testing purposes. In designing general oscillators, well-defined, stable oscillation frequency and amplitude are required. But an oscillator that is built from conversion of CUT is designed such that the variation of the components in CUT can be detected by measuring the oscillation frequency and amplitude.

$$H(s) = V\,o(s)\,/Vi(s)$$

$$= (a_2s^2 + a_1s + a_0) / (s^2 + b_1s + b_0) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where, $b_1 = \omega_0/Q$, and $b_0 = \omega_2$, ω_0 is the pole frequency, and Q is the pole quality factor that determines the distance of the poles on $j\omega$-axis in the s-plane. An infinite Q locates the poles on the $j\omega$-axis, and this can cause the circuit to oscillate. Therefore, in order for a filter to oscillate, the quality factor must be increased. First the Circuit component to be tested is converted into an oscillatory circuit by adding external circuitry in the feedback path so as to place a pair of poles of the system on the imaginary axis causing the system to become marginally stable causing oscillations. The concept of building of an Oscillator is explained in Fig. 3.

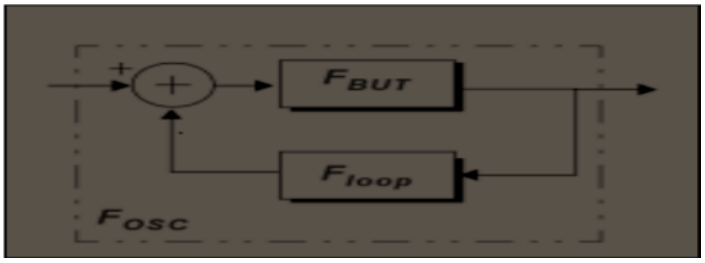


Fig 3. Concept of an building an Oscillator

4. General OBIST procedure

The test signals are sent into the system and the output from the normal mode and the faulty mode of the system are compared to create fault coverage. The General OBIST procedure is explained in Fig .4. Various faults are injected into the system such as removing a part of the circuit; Stuck faults etc. to cover the overall fault range.

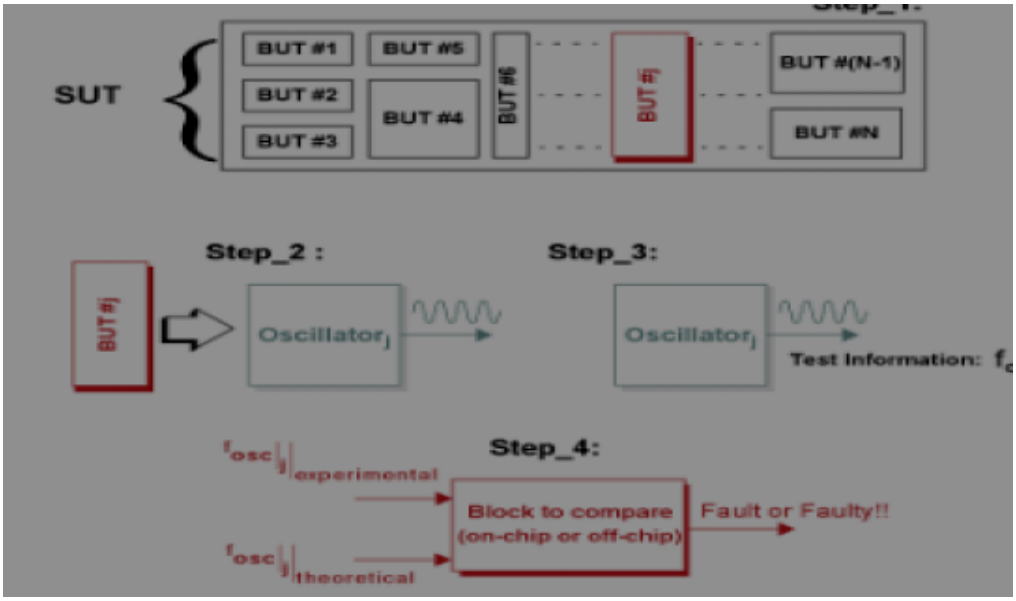


Fig .4. General OBIST Procedure

5. Concept of OBIST Strategy

A complex analog circuit is portioned into functional building blocks such as op-amps, filters, comparators, PLL etc. or a combination of these blocks. Each building block is converted into an oscillator by adding the proper circuitry in order to achieve sustained oscillation. The oscillation parameters are then evaluated. A faulty circuit is detected from a deviation of its oscillation parameters under fault free conditions. The oscillation parameters are independent of the CUT type and analog testing. The block diagram of OBIST strategy is explained in Fig .5.

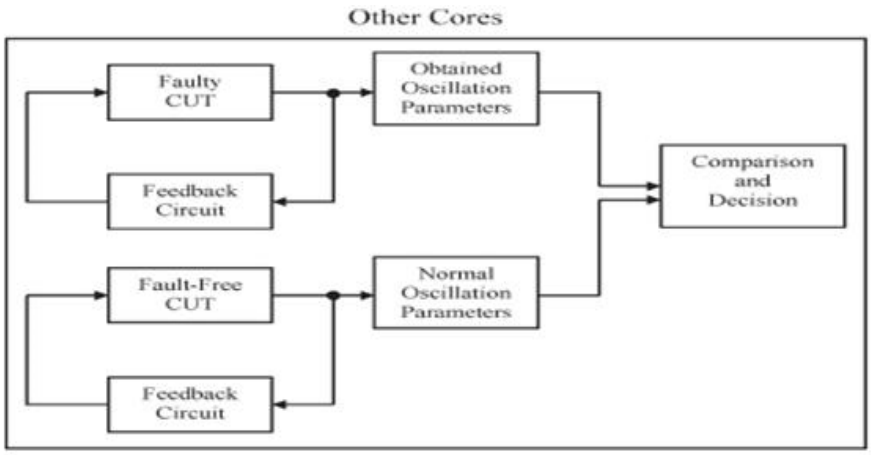


Fig .5. Block Diagram of OBIST Strategy

6. Analog Fault Modeling

Fault models for analog and mixed signal circuits can be classified into two categories. They are hard faults and parametric faults. A catastrophic fault is analogous to the stuck-at fault model in the digital domain where the terminals of the component can be stuck open or stuck-short. Parametric faults are deviations in component parameters that cause performance overshoot beyond acceptable limits. It is caused by statistical fluctuations in the manufacturing process. Catastrophic faults are introduced by random defects and results in failures in components. For example, dust particles on a photolithographic mask can cause either short or open in circuits or it may create large deviations of CUT parameters such as aspect ratio, threshold voltage change in a MOS transistor. These faults can be modeled as below in Fig.6. Stuck open faults are hard faults in which the component terminals are out of contact with the rest of the circuit. These faults can be simulated by adding high resistance in series. A Stuck- short fault is a short between the terminals of the component

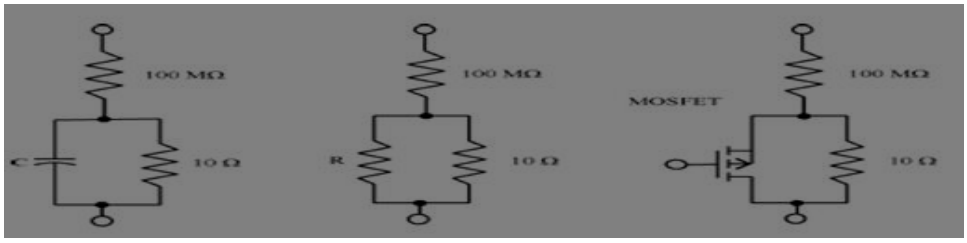


Fig .6. Stuck open and stuck short Fault Models for capacitor, resistor and MOSFET

7. Test Procedure

Parametric and catastrophic faults are injected into the circuit under test. These faults being injected into nominal circuit description are described in Spice format. By using Spice simulator transient and frequency domain response is evaluated. Fig.7.explains the test procedure for Oscillation based Built-in Self-test methodology. The different steps of the procedure are briefly given below.1. The fault free circuit is converted into an oscillator and simulated, and its test parameters are derived.

1. A fault list was derived from the CUT (circuit net list).
2. The faulty net list is generated (through fault injection).
3. A simulation was done for the faulty CUT.
4. The fault detection was completed on comparing the faulty-output measurements with fault-free test parameters.
5. The circuit fault coverage was calculated.

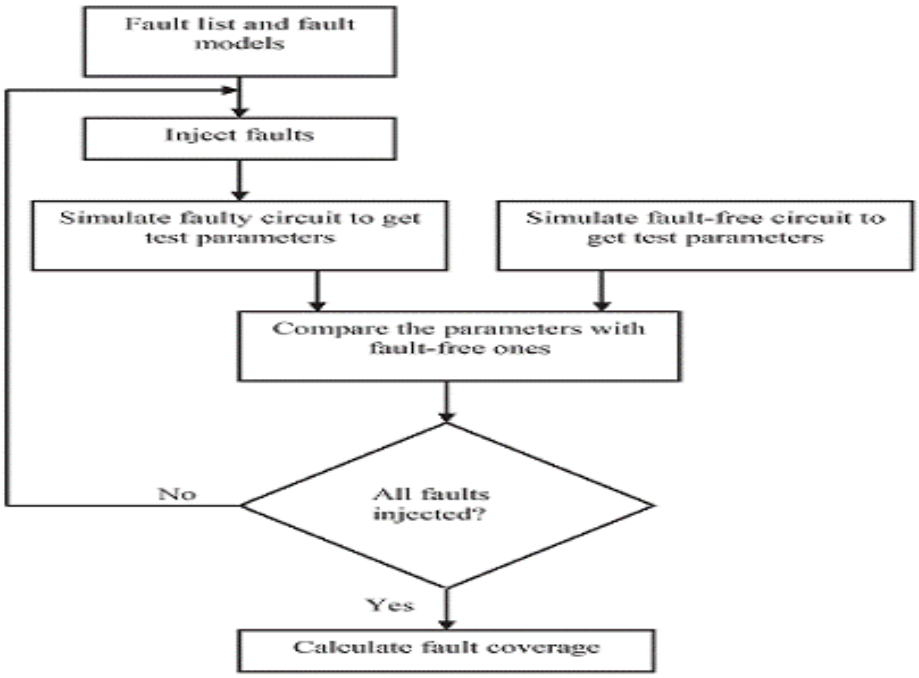
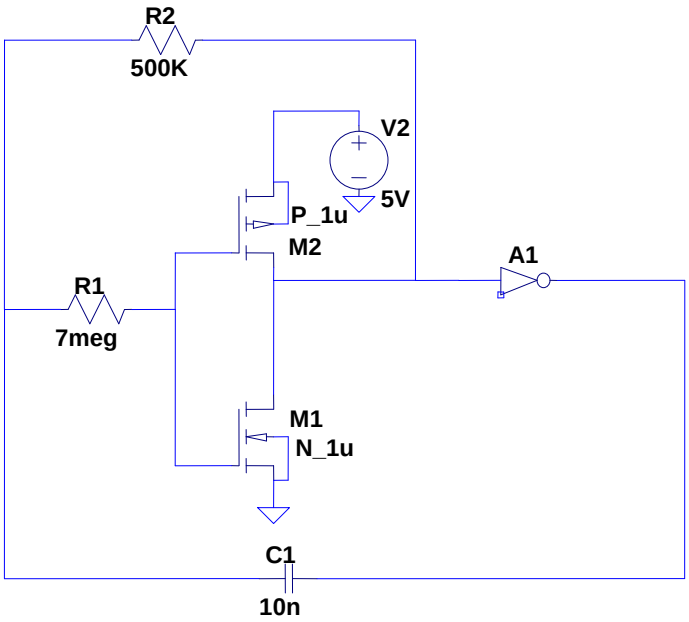


Fig.7. Test Procedure based on OBIST approach

8. Experimental Results

Purely analog ICs usually consist of amplifiers, comparators, PLL; filters etc., The test parameters specified by designers can be gain, signal to noise ratio, amplitude, power gain, phase shift, gain margin and phase margin and so on. Efficient ways to test the op –amps and filters are desired because of their importance in analog systems. In order to test any circuit with oscillation based method, first the circuit under test must be converted to an oscillator by adding extra circuitry as a feedback. If the circuit is faulty, converted circuit either won't oscillate or the response parameters of oscillation will differ from fault free condition. The proposed OBIST methodology for calculating the oscillation frequency is explained below (Fig. 8) by considering CMOS inverter as an example.



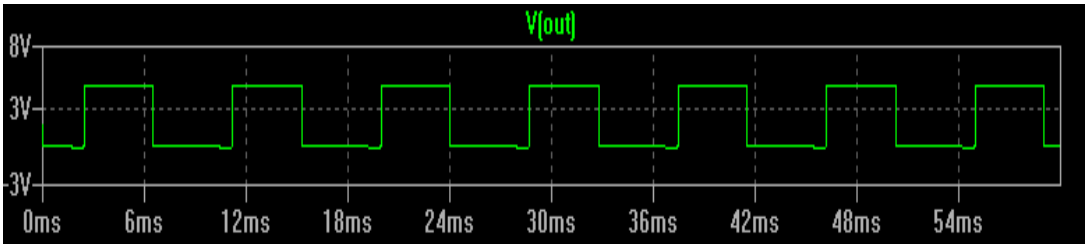


Fig.8.CMOS inverter as an oscillator and the output signal of CUT in test mode

By choosing R1 = 7MΩ, *C*1 = 10 nF, and *R*2 = 500KΩ, the oscillation frequency is calculated as *f*osc = 90.9 Hz. The Fig. 6. depicts the fault model for MOS transistors, where the value for the parallel resistor *Rp* is 100Ω, which emulates stuck short fault, and the series resistor *Rs* has a value of 100MΩ that emulates stuck-open fault. The output signal of the CUT in SPICE Simulation is shown in the Fig .8

Next, we consider the catastrophic (hard) fault injection in CUT in test mode. Injection of the below four faults specified in the CUT (inverter) in the test mode causes stopping of the oscillation of the circuit. If any one of the transistor is short or open, the output remains high or low according to the type of the fault. All the simulation results obtained below agree with this hypothesis.

Qn stuck-short

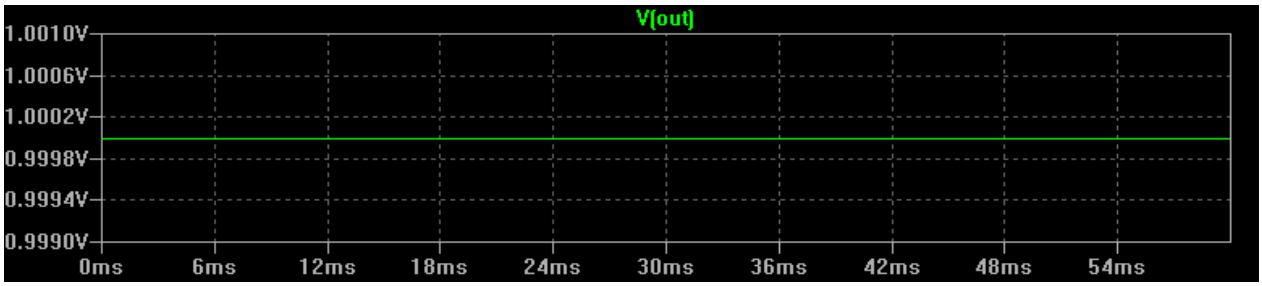


Fig.9. Output of CUT when Qn is stuck-short

We consider the stuck-short fault of NMOS Qn. Since the input of the second inverter shorted to ground node, the output will always be high. The same result has been obtained in SPICE simulation. The Simulation result is shown in Fig.9.

Qp stuck-short

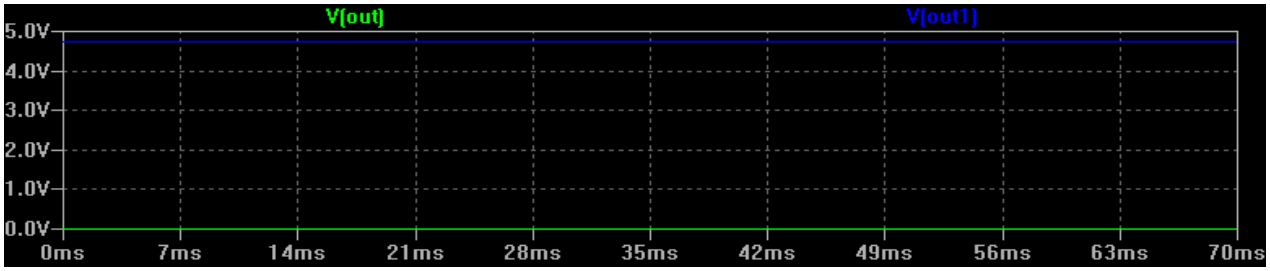


Fig.10. Output of CUT when Qp is stuck-short

A short fault is injected in PMOS transistor Qp. Since the input of second inverter is shorted to VDD, the output will always be zero. The same result has been obtained in SPICE simulation. The simulation result of output of CUT when Qp stuck- short is shown in Fig.10.

Qp stuck-open

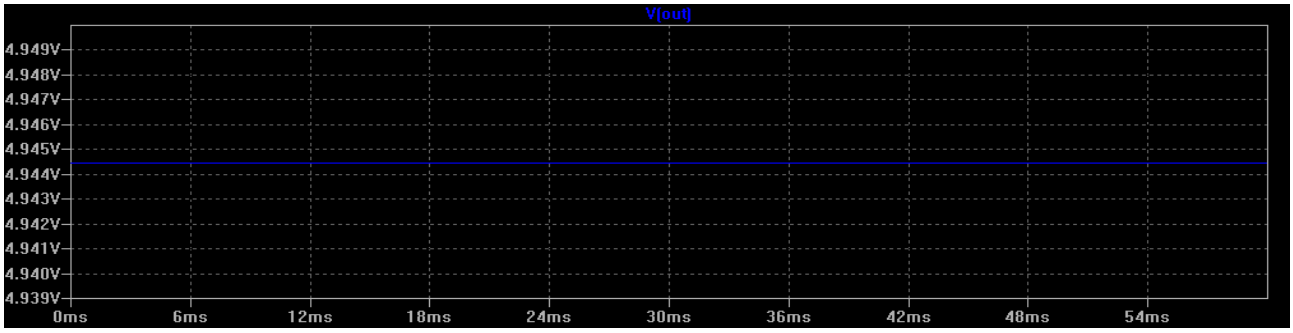


Fig.11. Output of CUT when Qp is stuck-open

A stuck- open fault is injected in Qp transistor, such that, it is disconnected from the remaining part of the circuit. The input of the second inverter is connected to the ground node. The output of second inverter turns high (near to 5V). A similar result is obtained with SPICE simulation. The Simulated result is shown in Fig.11.

Qn stuck-open

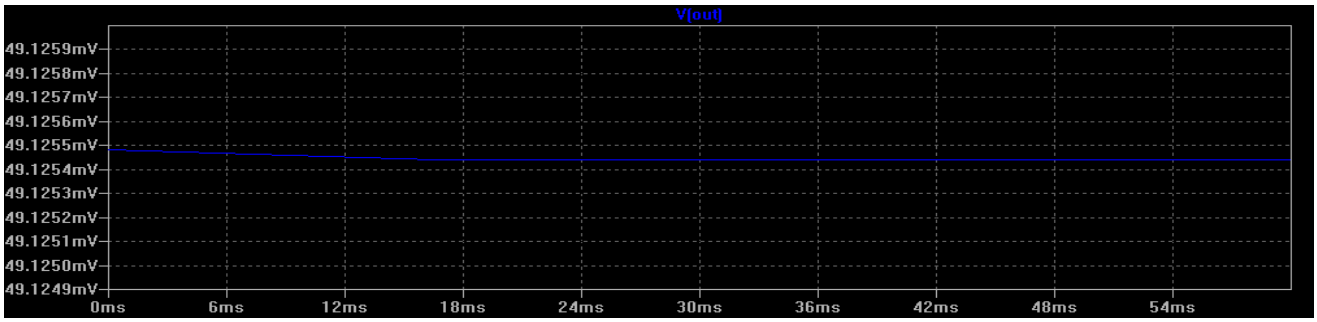


Fig.12. Output of CUT when Qn is stuck-open

A CMOS inverter is converted into astable oscillator using one more inverter and one RC feedback. Qn is disconnected from the remaining part of the circuit. The input of the second inverter goes high from VDD. So the output of that inverter goes low. The same result obtained in SPICE Simulation. The simulated result is shown in Fig.12

FET Oscillator in test mode

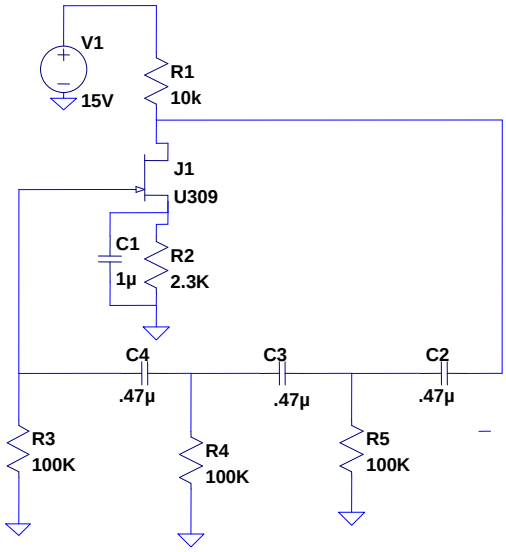


Fig.11. FET Oscillator in test mode

Table 1. The FET Oscillator faults and fault coverage analysis

Faults	Amplitude	BW (Hz)	Power BW (Hz)
R1 short	14.9V	268.50	**42.360**
R2 short	92.7mV	269.76	**42.340**
R5 short	7.70 V	268.36	**42.603**
C2 short	7.07V	270.24	**42.699**
C4 short	8.00V	126.90	**19.860**
R4 short	7.77V	268.36	**42.600**
R3 short	7.775V	267.36	**42.603**
R3 open	7.767V	268.36	**42.600**
Fault free	**14.80V**	**107.10**	**18.804**

Table.1 presents the results obtained by spice simulation for FET oscillator when the hard faults are injected. FET Oscillator produces oscillation frequency without fault as fosc = 1.45 KHz. By injecting short faults in the circuit, the FET operates in cutoff region. When the FET is open, it is disconnected from the circuit does not oscillate. Fault is detected when the power bandwidth is out of a tolerance band, defined as ±5% of the fault free power bandwidth to get nominal fault coverage.
Fault free power BW= 18.804Hz.
Threshold band range =19.1742-17.8638Hz.
Here, all the possible faults present in the circuit have not been considered. For the faults considered, 100% fault coverage was achieved.

Single Op-amp oscillator

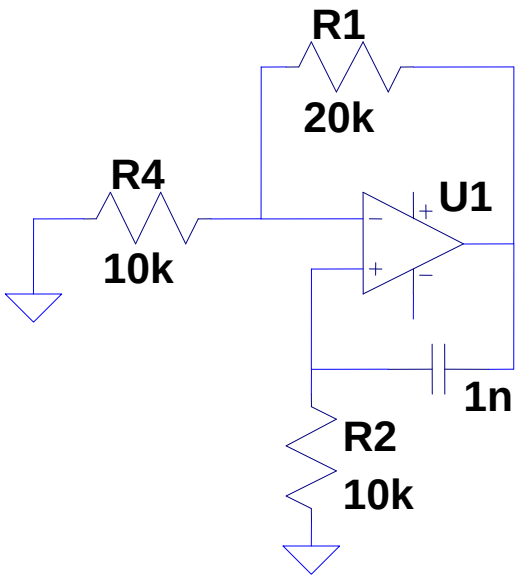


Fig.12. Single Op-amp Oscillator

As given in Fig.12. an op-amp is converted to an oscillator by adding both positive and negative feedback. In a fault free case, the oscillation frequency is fosc= 9 KHz. The results of parametric analysis of single Op-amp oscillator is displayed in time domain and frequency domain Fig.13 and Fig.14.This oscillation frequency significantly varies with any hard or parametric faults injected into the circuit. To improve the fault coverage, both amplitude and frequency measurements are to be considered. The parametric test analysis on this circuit, when analyzed indicated significant frequency deviation in the value of R and C. Changing different components in different parts of the circuit shows different effect on the output response. For example, changing the value of capacitor in the circuit from 1n to 100n resulted in a drastic change in the output frequency value. It has been shown in Fig.15. This was completely away from the desired range of frequency. It confirms that different components have different sensitivity.

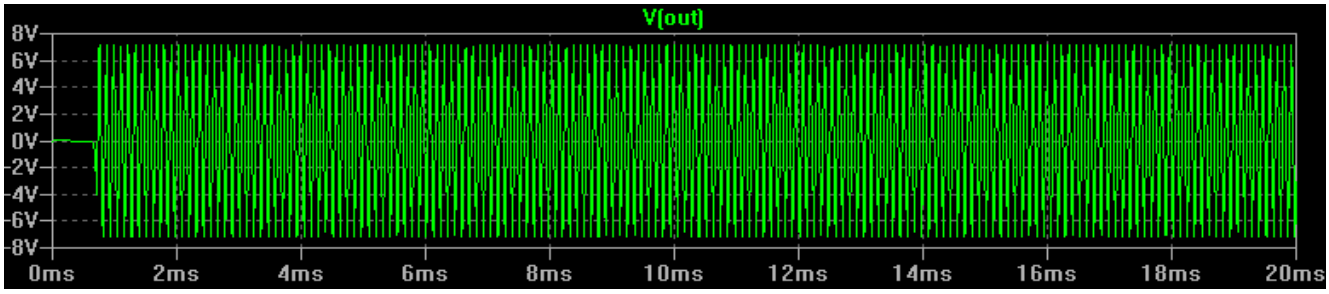


Fig.13. Simulation result in time domain for a single Op-amp oscillator

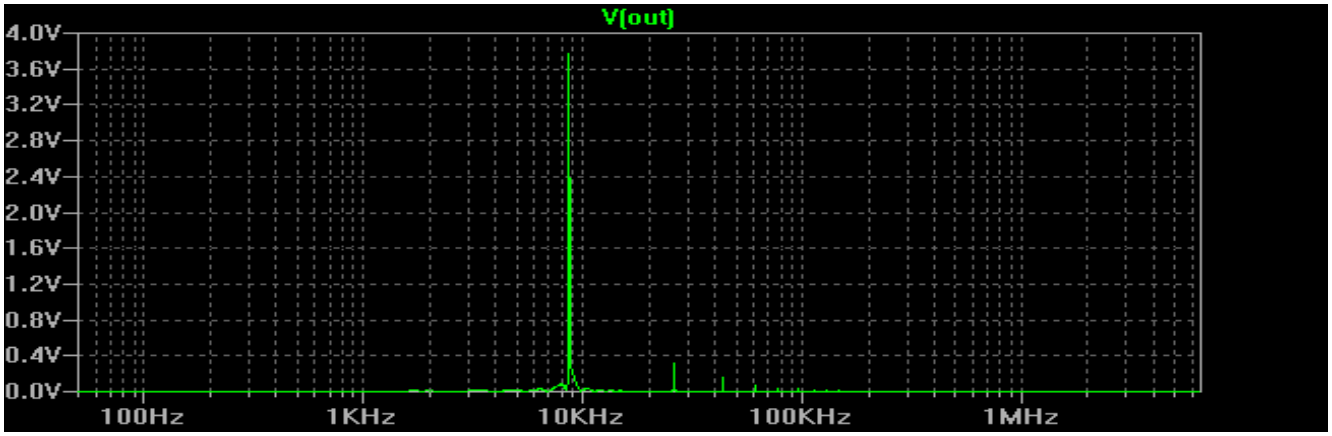


Fig.14. Simulation result in frequency domain for a Single Op-amp oscillator

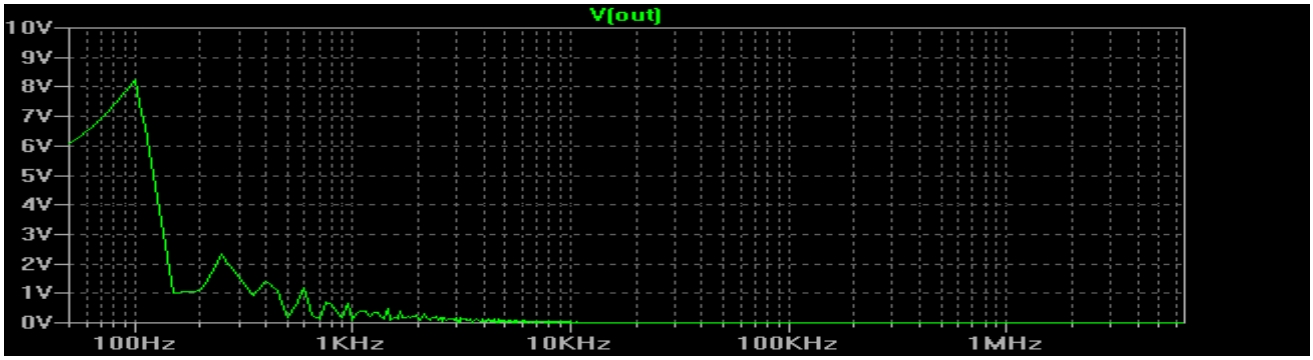


Fig.15. Simulation result for C1 parametric

9. Conclusion

The OBIST method has been effectively employed in testing and mixed signal circuits in embedded core based SOC environments. There are many ways to ensure proper functioning of a designed circuit, but this built-in hardware approach has proven to be one of the most reliable method. This oscillation based technique is implemented where the hard and parametric fault models are defined for fault coverage evaluation. By using Amplitude and Frequency measurement together we have seen improvement in fault coverage. Some sample benchmark circuits have been simulated and studied. The results have been verified in spice Simulation Software. The detection of faults in fault coverage shot up when the TIME-DOMAIN output was converted to FREQUENCY-DOMAIN and compared with the same ±5% threshold values. A very high coverage of 100% was achieved as well. The OBIST methodology has been applied for many circuits like analog to digital converter, filters, Dual tone multifrequency Detector, Switched Capacitor circuits and even MEMS systems.

References

[1] M. J. Ohltz, "Hybrid built-in self-test (HBIST) structure for mixed analog/digital integrated circuits ", in Proc. Eur. Test Conference, 51-57, 1991.

[2] Karim Arabi and Bozena Kaminska, "Oscillation-Test Methodology for Low-Cost Testing of Active Analog Filter", IEEE Transactions and Instrumentation and Measurement, August 1999.

[3] S. R. Das, "Self-testing of embedded cores-based systems with built-in hardware", *Proc. Inst. Electrical. Eng.—Cir. Dev. Syst.*, vol. 152, no. 5, 539–546,March 2005.

[4] S. Sedra and K. C. Smith, '*Microelectronic Circuit,* 2nd ed. New York: Holt, Rinehart, and Winston, 1987

[5] Sunil.R.Das,j et.al, June, "Testing Analog and Mixed –signal circuits with Built-in Hardware-A New Approach", IEEE Transactions On Instrumentation And Measurement, vol. 56, no. 3, 840-852, June 2007.