DESIGN OF PULSE TRIGGERED FLIP FLOP USING PULSE ENHANCEMENT SCHEME

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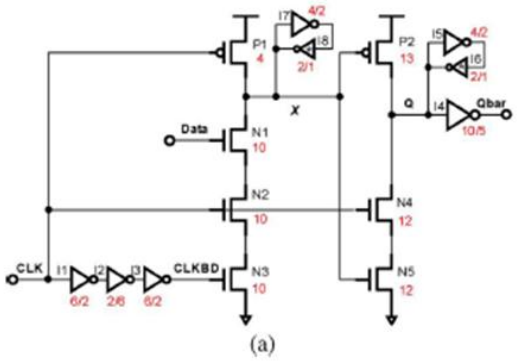
Abstract
For the past several years, much progress has been made in Low power VLSI Design .In This paper ,a novel low-power pulse Triggered flip- flop design is presented. First, the pulse generation control logic an AND function, is removed from critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the proposed design features the best power-delay-product performance in four FF designs under comparison.

Keywords: Flip flop, low power and pulse-triggered

I Introduction
Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power[1]. In recent VLSI's, a clocking system, including clock interconnections and flip flops. This is partially because the activation ratio of a clock system is unity. In this clocking system power, 90% is consumed by the last branches of the clock distribution network which derive directly F/F's and the F/F's themselves. P-FF has been considered a popular alternative to the conventional master-slave based FF in the application of high speed operations[2]. High performance flip flops are key elements in the design of contemporary high-speed integrated circuits. In these circuits, high clock frequencies are generally gained by using a fine grain pipeline in which only few logic levels are inserted between pipeline stages. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

II Implicit-Type P-FF Design With Pulse Control Scheme
Conventional Implicit-Type P-Ff Designs:

1. ip-DCO
Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a) [6]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on.



(a)

Fig. 1(a) ip-DCO

2. Mhllf:
An improved P-FF design, named MHLLF Fig.1 (b) MHLLF, by employing a static latch structure presented in [10]. Node is no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data

both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".

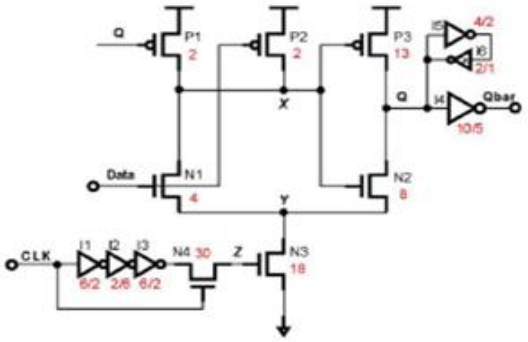


Fig. 1(b) MHLLF

3. SCCER:

A refined low power P-FF design named SCCER using a conditional discharged technique [9], [8]. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node [8]. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged.

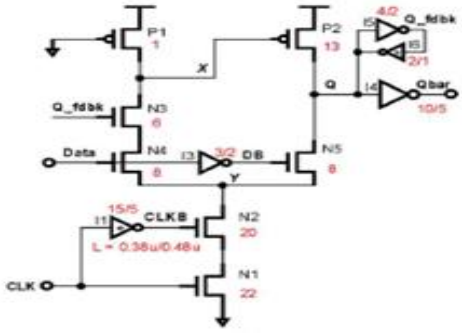


Fig. 1(c) SCCER

This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

III Simulation Results

A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation.

To demonstrate the superiority of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the three P-FF designs shown in Fig. 1 (ip-DCO [6], MHLLF [9], SCCER [10]), another P-FF design called conditional capture FF (CCFF) [7], and two other non-pulse-triggered FF designs, i.e., a sense-amplifier-based FF (SAFF) [2], and a conventional transmission gate-based FF (TGFF). The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V. Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation. All designs are further optimized subject to the tradeoff between power and D-to-Q delay, i.e., minimizing the product of the two terms.

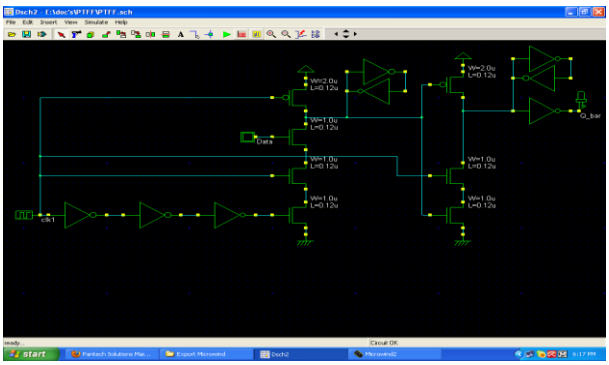


Fig. 2(a) ip-DCO in Microwind

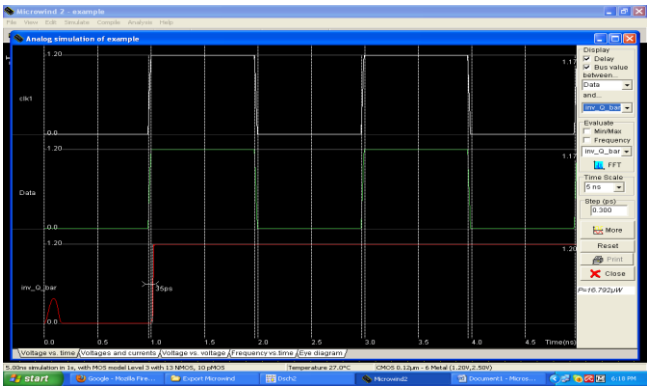


Fig. 2(b) ip-DCO waveform in Microwind

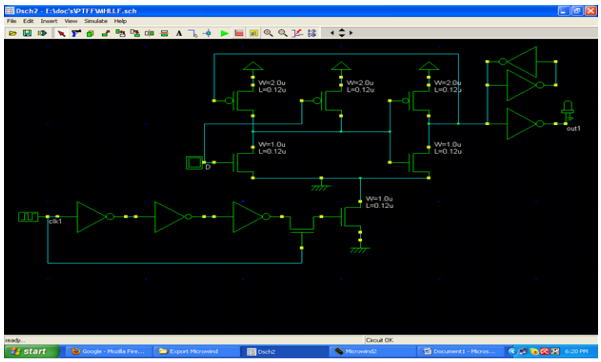


Fig. 2(c) **MHLLF** in Microwind

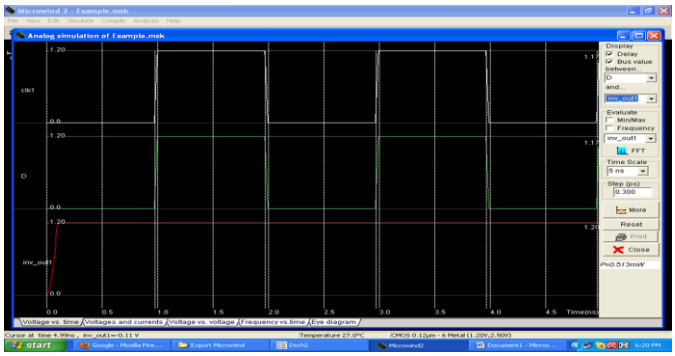


Fig. 2(d) **MHLLF** waveform in Microwind

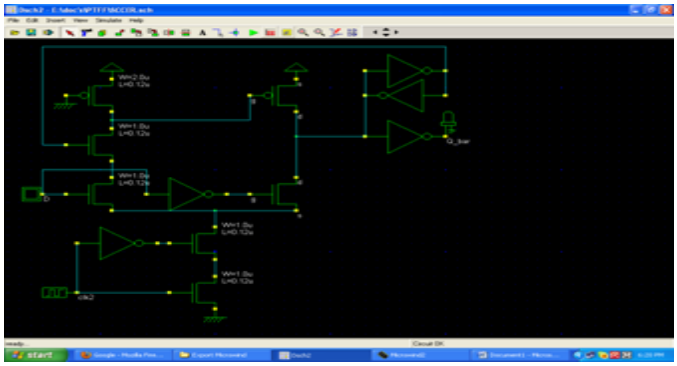


Fig. 2(e) SCCER in Microwind

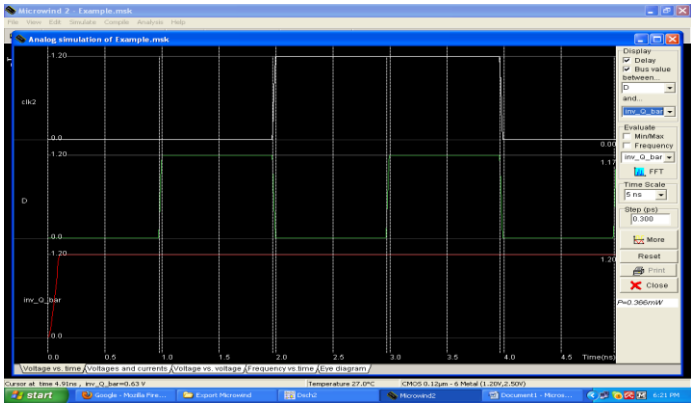


Fig. 2(f) SCCER waveform in Microwind

These are the simulation block and its results of ip-DCO, MHLLF and SCCER in Microwind.

IV Comparison Table

P-FF	ip-DCO	MHLLF	SCCER
No of transistors/lay out area(μm^2)	23/91.88	19/93.02	17/80.07
Average power(µw)	42.20	35.96	36.27
Optimal power delay product	4.22	4.89	3.19

Table: 1 Comparison of designed methods

From the designed methods the various parameters are tabulated and compared. With this comparison results the SCCER performed better than other two designed methods.

V Conclusion

In this paper, the various Flip flop design like, ip-DCO, MHLLF and SCCER are discussed. These were been also designed in Wicrowind tool and those result waveforms are also discussed. The comparison table also added to verify the designed methods. With these all results SCCER performed better than ip-DCO and MHLLF designs.

VI Future work

To improve the performance design of the P-Flip flop, The Pulse enhancement scheme will be designed and also these results will be discussed with the existing pulse trigger Flip Flop.

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