A Fast Gain Stage Suitable for High Performance Pipeline ADCs

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Abstract- A new circuit technique for voltage gain enhancement in CMOS op amp design suitable for low voltage and high speed operation is presented. In this paper, a new operational amplifier is presented that improves the specifications such as dc gain and speed virtually .To obtain these improvements, we have used the two important concepts of positive feedback and replica amplification.

Keywords: Replica amplification, positive feedback, Gain-Bandwidth-product (GBW), single stage amplifier

1. Introduction

Op Amps play an important role in many analog and mixed-mode applications. The rapid growth of high speed and high-resolution applications such as ADC and DAC's results in a necessary demand to the high speed and high gain amplifiers. The realization of high-gain amplifiers with large GBW in processes with decreasing supply voltage requires innovative circuit design techniques and advances in IC process technology. Since op amps are usually employed to implement feedback systems, the open-loop gain of an op amp determines the precision of the feedback system employing the op amp. With a very high dc gain needed for precision applications, four approaches for gain enhancement has received considerable attention for many years. One is based upon gain multiplication achieved by cascading two or more lower gain stages. Although high dc gains are achievable, the excess phase shift introduced by the cascading introduces serious compensation requirements which limit the high frequency performance of cascaded amplifiers in feedback applications. The second approach achieves gain enhancement by increasing the output impedance of a basic gain stage. This approach has proven most effective at achieving high gains and high GBW with favorable power dissipation (for medium accuracy). E. H. Armstrong, first time, in 1914, presented positive feedback [1] and this method, several times, was used in op-amps. Using positive feedback, dc gain can be increased a lot, but it simply, can make op-amp structures unstable. Also, this method can decrease output swing the same as negative feedback in active cascode op-amps [2]. Another commonly used gain enhancement technique is gain-boosting [3]. Very high gains are achievable with gain-boosting but it still requires one level of stacking of devices thereby making it difficult to operate with low supply voltages. The gain-boosting amplifier also adds its own poles, and reduces the speed of amplifier and consumes more power. Although negative impedance compensation offers potential for the most gain enhancement, low power dissipation, low voltage operation and excellent high frequency performance, the technique is seldom used commercially because of the high sensitivity of the gain to the negative compensating impedance inherent in existing negative impedance schemes. In 1993, a new concept as replica amplification was introduced [4]. This method is more suitable for low voltage and high performance applications such as data converters. We have designed an op amp by using this method.

2. Circuit design

2.1 Single Stage amplifier

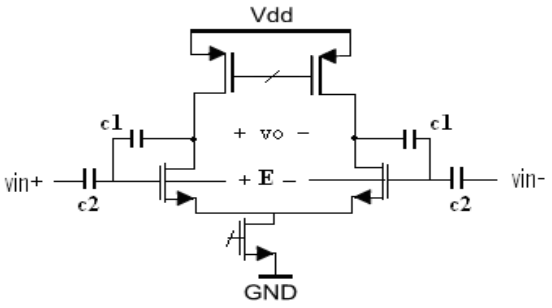
The single stage amplifier having one pole is the simplest architecture imaginable. Because of its simplicity, it can be extensively analyzed and optimized by hand analysis. The single pole amplifier is also of a great deal of interest because of its inherent stability. The simple single pole architecture makes this amplifier the most attractive for high speed applications with low closed loop gain. We have improved the dc gain of single stage amplifier by using replica method. This method (replica) has a negligible effect on settling time of main amplifier [4].There is not any GBW limitation, in this method. Fig. 1a shows the single stage amplifier with active load in closed loop configuration. The dc-gain of this structure (intrinsic gain) in the 0.35 μm CMOS process can be about 10 to 30 depend on devices size and input signal range. But by using negative impedance gain-enhancement (fig. 1b) we can increase the dc-gain (Av) of single stage amplifier a little, without any stability problems [5]. In this design gain enhancement by this technique is used to be 2. This structure has only one pole that's located in the output node. Therefore the speed of this circuit is high.

2.2 Replica Method:

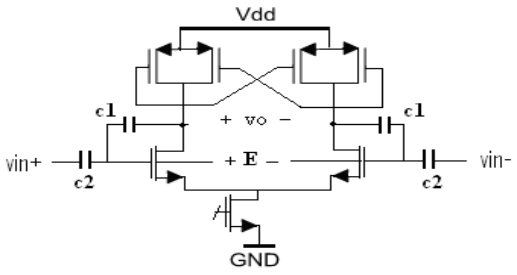
Replica amplification is an ideal method for enhancing amplifiers dc-gain virtually, without any GBW limitation. This idea for the first time has been used in a two stage op amp structure [4]. Measurement results of fabricated circuit in [4] show the excellent improvements of replica method.

2.3 Proposed Circuit

Fig. 2 shows the complete schematic of the designed circuit. The total closed loop gain of this structure is designed to be one but with scaling the feedback capacitors (c1 and c2) we can achieve more different gains, especially for the residue amplifiers in the Pipeline ADC's. The structure is consists of a main and a replica amplifier. Output voltage and error (indeed error of a single stage amplifier) of replica amplifier can be estimated by:



(a)



(b)

Fig. 1: Simple single stage amplifiers.

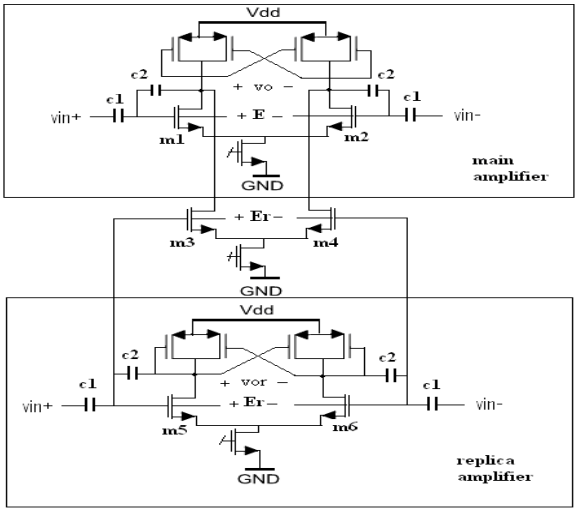


Fig.2 Proposed design

$$V_{Or} = \frac{A_{Vr}.V_{in}}{(1+A_{Vr})} \qquad (1)$$

$$E_r = \frac{V_{in}}{(1+A_{Vr})} \qquad (2)$$

This error voltage appears in the gates of the input differential pair (m5, m6). The main idea is to amplify the error by using another differential pair (m3, m4) that is connected directly to the output nodes of main amplifier. The load of this differential pair is output impedance of main amplifier. The gain of this amplification ($Av_{s.}$) can be equal to Av_r by scaling the size of the devices (m3, m4) as well. Using this method, output voltage of the main amplifier can reach to Vo_r only by replica amplifier

and an extra differential pair (m3, m4) (without any effect of the main amplifier). The main amplifier only corrects the difference of V_{in} and Vo_r (E_r) and decreases it to the final error (E). Assume Av_s is equal to Av_r, the total error of complete amplifier (E) that appears between the gates of input differential pair of the main amplifier is equal to:

$$E = \frac{E_r}{(1+A_{Vm})} = \frac{V_{in}}{(1+A_{vm}).(1+A_{Vr})} \qquad (3)$$

Where Av_m is the dc gain of the main amplifier. Hence the total error of the amplifier is reduced and the circuit can be more accurate. The speed improvement in this method has another reason too. The size of the feedback capacitors in the other gain enhancement methods (e.g. in the gain boosting method), must be large enough for capacitor matching (needed for desired accuracy), especially to compensate the parasitic capacitance effect of the gates of the input differential pair that alters the accuracy of the amplifier. And these large capacitors increase the settling time of the circuit. But in this design the feedback capacitors can be smaller, because each of the main or replica amplifiers needs less accuracy (half of the total desired accuracy). Using smaller feedback capacitors increase the speed of the circuit more and more. The circuit of Fig. 3 can be used for more precision. In this circuit the replica method is used twice so this topology can be more accurate if well designed, only by scaling the size of the devices (without any reduction in output impedance of the main amplifier). This configuration has never been reported yet. Using replica method for two times is another novel idea in this research. In this way instead of cascading or cascoding stages to achieve high dc gain that leads to speed reduction in the closed loop configuration, we can use more replica stages (replicating) to achieve more accuracy with a very small reduction in speed [4]. This speed reduction is only 20% that reported in [4] and can be reduced by scaling down of replica amplifier. In the circuit of fig.3, for every stage of the amplifier we can use the circuit of fig.1 (b) for more gain enhancement.

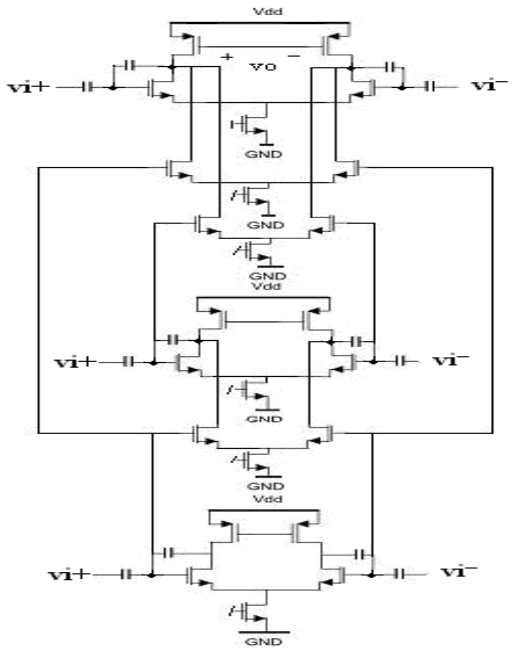


Fig. 3 More gain enhancement by replica method.

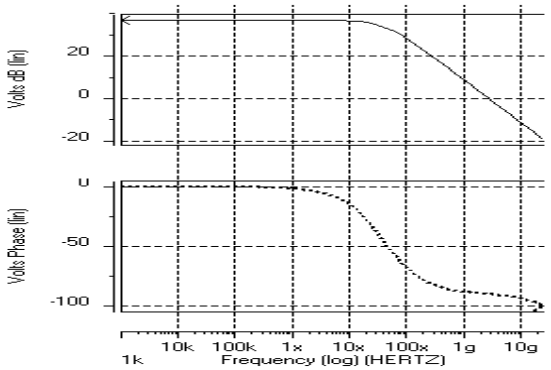


Fig.4 Ac response of single stage op-amp (circuit of fig. 1b)

3. Simulation results

The circuit of fig.2 is simulated by Hspice software using level 49 parameters (BSIM3v3). Fig.4 shows the AC response of designed amplifier (shown in fig.2). The step respons of circuit is shown in fig.5. The size of feedback capacitors is 0.5pF and a 0.5pF capacitive load is connected to the output nodes. Power dissipation of circuit is about 6mW.The settling time of the circuit for 0.1% error is less than 2nsec and that is depend on the amplitude of input signal, feedback and load capacitors size and bias currents 4]. Replica concept has been analyzed in detail in [4].

4. conclusion

A new circuit technique for voltage gain enhancement in CMOS op amp design suitable for low voltage and high speed operation is presented. In this paper, a new operational amplifier is presented that improves the specifications such as dc gain and speed virtually .To obtain these improvements, we have used the two important concepts of positive feedback and replica amplification. Indeed by using this method we can design an op-amp with accuracy of two stage op-amp but with speed of a one stage op-amp.

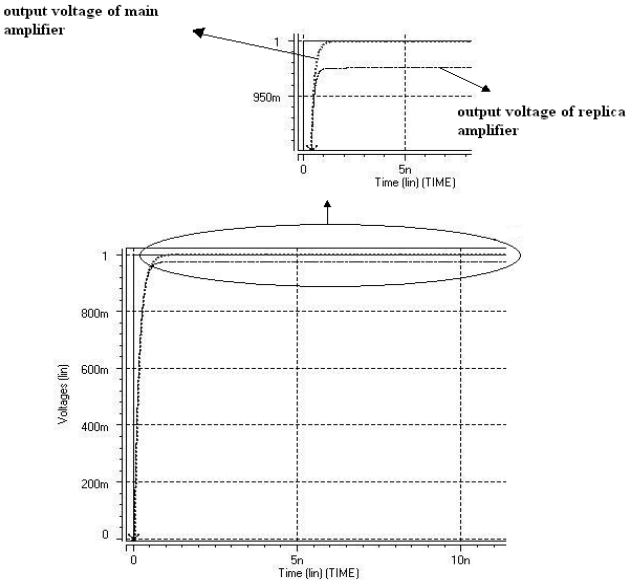


Fig.5 : Step response of proposed design.

Table 1: Op Amp Performance

Supply voltage	3.3v
process	0.35 μ m
Power Dissipation	$\approx$ 6mW
Load (pF)	0.5
0.1% error settling time In 1 volt step voltage	Less than 2 nsec
DC Open loop gain (virtual)	$\approx$ 1000
Phase margin	$\approx 90^0$

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